UNIT-1

Syllabus ⇒

Operational amplifier fundamentals ⇒

- ✓→ Basic op-amp ckt.
- ✓→ op-amp parameters
  - ✓→ i/p & o/p voltage.
  - ✓→ CMRR.
  - ✓→ PSRR.
  - ✓→ offset vtgs and currents.
  - ✓→ i/p & o/p impedance.
  - ✓→ slew rate
  - ✓→ frequency limitations.

Sd/-
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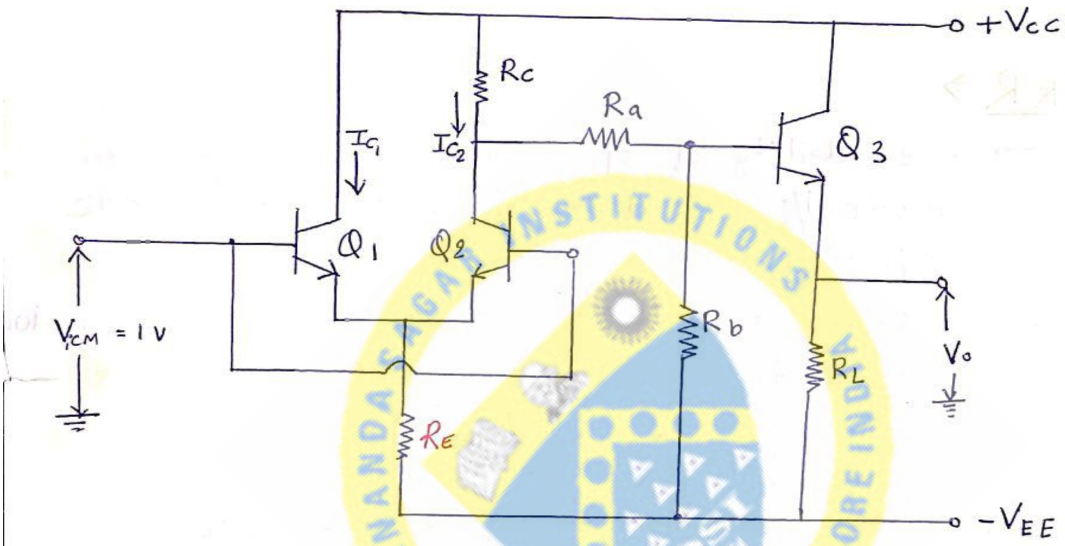
Op-amp as DC amplifiers ⇒

- ✓→ Biasing Op-amps.
- ✓→ Direct coupled
  - ✓→ Voltage follower
  - ✓→ NON-INV ampr
  - ✓→ INV ampr
  - ✓→ Summing ampr
  - ✓→ Difference ampr.

P-1

Q.1. Explain common-mode voltage, common mode voltage gain and common mode rejection ratio for operational ampr. Show that $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \times A_v$. (10M)

⇒



Common-mode voltage ⇒

→ The two input terminals are shorted together & a dc vtg $V_{icm} = 1V$ is applied. This is known as a common mode input.

→ For common mode i/p, o/p ideally should be zero.

Common-mode voltage gain ⇒

→ Since base voltages of Q_1 & Q_2 are raised by 1V, the voltage drop across R_E also increases by 1V. This increases I_{C_1} and I_{C_2}. Thus vtg drop across R_C also increases, which results in a change in o/p.

→ similarly, if a −1V common mode i/p is applied, I_{C_2} falls and again a change is produced at o/p.

→ Thus, Common-mode voltage gain is defined as the ratio of change in o/p vtg to change in common mode i/p vtg.

i.e. $A_V = \frac{V_{o(cm)}}{V_{i(cm)}}$

CMRR ⇒

→ The ability of op-amp in rejecting common mode i/ps is defined as common mode rejection ratio (CMRR).

→ CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain Acm.

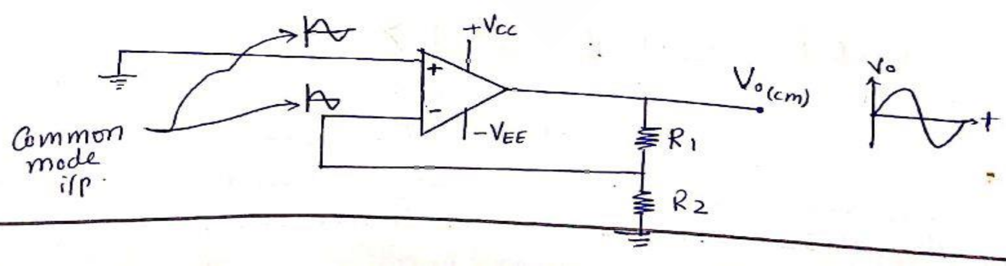
i.e. $CMRR = \frac{M}{A_{cm}}$

→ CMRR is usually expressed in decibels.

$$(CMRR)_{dB} = 20 \cdot \log_{10}\left(\frac{M}{A_{cm}}\right) \text{ dB}$$

→ Typical value of CMRR for 741 IC is 90 dB.

Proof of the expression ⇒



WKT.

V_d = differential i/p vtg:

$$= \frac{V_{ocm}}{M} \qquad \therefore \left\{ \frac{V_{ocm}}{V_{icm}} = A_{cm} \right\}.$$

$$= \frac{A_{cm} \times V_{icm}}{M} \quad \text{——— (1)}$$

But, V_d is the feedback developed across R_2 due to potential divider action:

$$\therefore V_d = V_{ocm} \cdot \frac{R_2}{R_1 + R_2}$$

$$= \frac{V_{ocm}}{\left(1 + \frac{R_1}{R_2}\right)}$$

$$= \frac{V_{ocm}}{A_v} \quad \text{——— (2)} \qquad \therefore \left\{ \left(1 + \frac{R_1}{R_2}\right) = A_v \right\}.$$

Equating eqn (1) and (2)

$$\frac{A_{cm} \times V_{icm}}{M} = \frac{V_{ocm}}{A_v}$$

$$\Rightarrow \frac{V_{ocm}}{A_v} = \frac{V_{icm}}{\left(\frac{M}{A_{cm}}\right)}$$

$$\Rightarrow V_{ocm} = \frac{V_{icm}}{\left(\frac{M}{A_{cm}}\right)} \times A_v$$

We know that;

$$\frac{M}{A_{cm}} = CMRR.$$

$$\therefore \boxed{V_{ocm} = \frac{V_{icm}}{CMRR} \times A_v}$$

Q.2. Define slew rate and unity gain bandwi[dth]. What is the effect of slew rate on the output voltage of an op-amp. (6M)

⇒ Slew rate ⇒

→ The slew rate 's' of an op-amp is the max^m rate at which the o/p vtg can change.

→ When the slew rate is too slow for the i/[p], the o/p will distort.

$$\text{Slew rate} = \frac{\Delta V}{dt} \quad \text{or} \quad S = \left.\frac{dV_o}{dt}\right|_{max}$$

→ Typical value for 741 op-amp is 0.5 V/μsec

Unity gain-bandwidth ⇒

→ The gain band-width product or unity gain band-width of an op-amp is the closed loop gain A_v multiplied by the cut-off frequency for that gain.

$$A_v . f_2 = f_u \quad \text{or} \quad f_2 = \frac{A_v}{f_u}$$

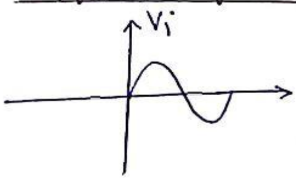
where,

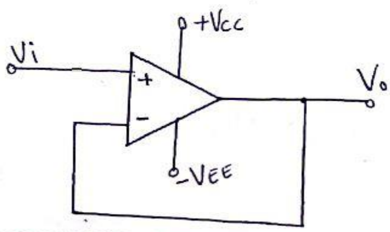
f_u = unity gain freq.

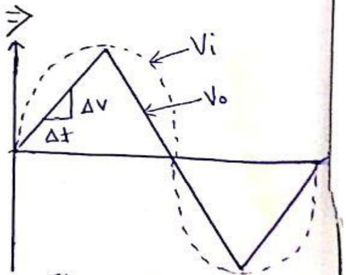
A_v = closed loop gain.

f_2 = cut-off freq.

Effect of slew rate on o/p of op-amp ⇒







Slew rate = $\frac{\Delta V}{\Delta t}$.

→ let us consider a voltage follower, applied with sine wave input.

→ when the i/p vtg changes too fast, the output waveform distortion results. i.e when 'S' is too slow for i/p results in distortion.

→ This is shown above a sinusoidal i/p produces a triangular o/p in a voltage-follower ckt.

Q.3. Explain dc - two i/p inverting summing ampr with neat diagram and necessary design steps.

⇒

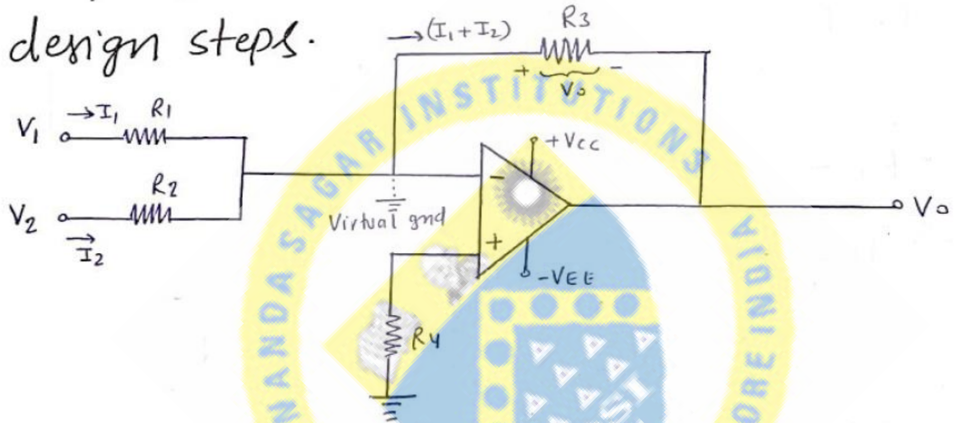


Fig. op-amp inv summing ampr ckt with 2 i/ps.

→ Fig. shows a ckt that amplifies the sum of two or more i/ps.

→ Since the inverting terminal behaves as a virtual ground, the currents through resistors R_1 & R_2 are respectively given by:

$$I_1 = \frac{V_1}{R_1}, \&$$

$$I_2 = \frac{V_2}{R_2}$$

→ These two currents flows through R3.

Applying KVL from R3 to o/p:

$-(I_1 + I_2) R_3 - V_o = 0$

$\Rightarrow \boxed{V_o = -(I_1 + I_2) R_3} \longrightarrow (1)$

→ substitute I_1 and I_2 in equn (1).

$V_o = -R_3 \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right]$

$\Rightarrow V_o = \frac{-R_3}{R_1} [V_1 + V_2]$ ∴ [With $R_1 = R_2$]

But, $A_V = -\frac{R_3}{R_1}$

$\Rightarrow \boxed{V_o = +A_V (V_1 + V_2)} \longrightarrow (2)$

→ If $R_1 = R_2 = R_3$, then $A_V = -1$

∴ $V_o = -1 \cdot (V_1 + V_2) \Rightarrow \boxed{V_o = -(V_1 + V_2)}$.

→ $R_4 = R_1 || R_2 || R_3$.

→ The o/p voltage is given by:

$$\boxed{V_o = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right] R_4}$$

<u>Design</u> ⇒

(1) $I_{1\,min} = 100 \times I_{B\,max}$

(2) $R_1 = \frac{V_{s\,min}}{I_{1\,min}}$

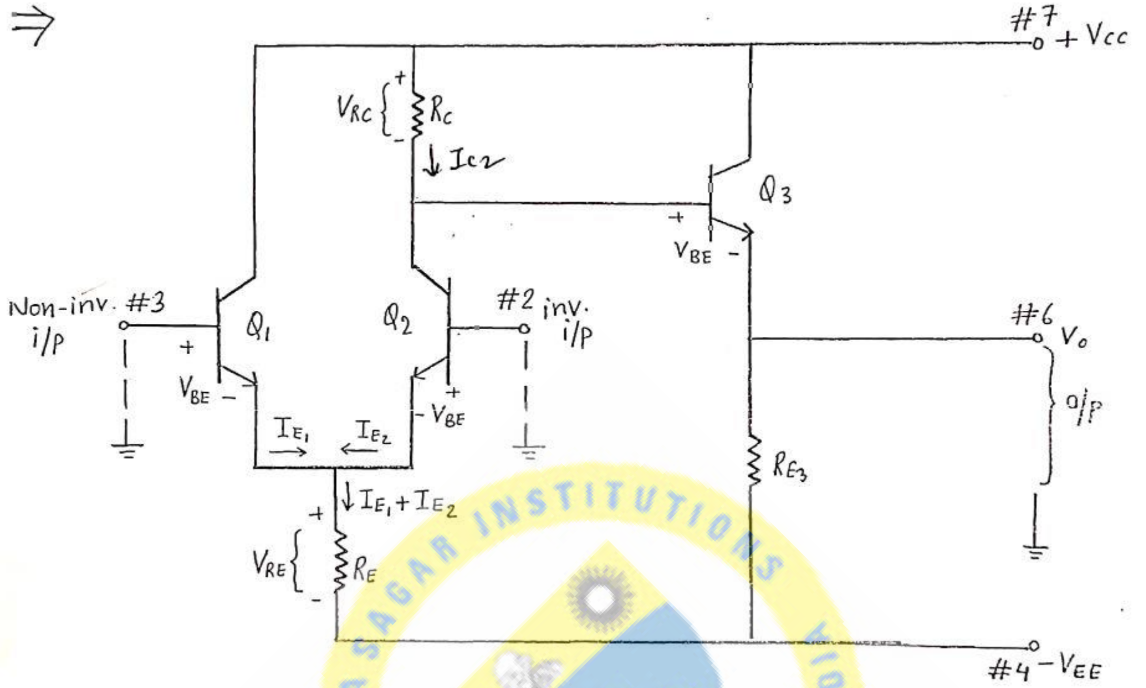
(3) $R_1 = R_2$

(4) for, $A_V = -1$, $R_1 = R_3$

(5) $R_4 = R_1 || R_2 || R_3$

Q1. Explain the basic operational ampr circuit with neat diagram.

⇒



→ Basic circuit of an operational ampr has a differential ampr i/p stage & an emitter follower o/p.

→ It is provided with $+V_{cc}$ & $-V_{EE}$ supply voltages and the two i/p terminals are grounded.

→ Transistor Q_1 & Q_2 forms a differential amplifier.

→ When a difference i/p voltage is applied to the bases of Q_1 & Q_2, it produces a voltage change at the collector of Q_2.

→ Transistor Q_3 acts as emitter follower to provide a low o/p impedance.

→ The dc o/p voltage at pin 6 is
(applying KVL from Vcc, Rc, Q3 base & o/p, we

$$V_{cc} - I_{C_2}R_C - V_{BE_3} - V_o = 0$$

$$\Rightarrow \boxed{V_o = V_{cc} - I_{C_2}R_2 - V_{BE_3}}$$

→ Assuming that Q_1 & Q_2 are matched (Identical) transistors, which provides equal V_{BE} levels & current gains.

→ With both transistors bases at ground level, the emitter current I_{E_1} & I_{E_2} are equal & flow through common emitter resistor 'R_E'.

→ The total emitter current is given by:

$$I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$$

→ Applying KVL from base of Q_2 to $-V_{EE}$ supply:

$$-V_{BE} - (I_{E_1} + I_{E_2})R_E + V_{EE} = 0$$

$$\Rightarrow \boxed{I_{E_1} + I_{E_2} = \frac{V_{EE} - V_{BE}}{R_E}}$$

Case-I.

→ To investigate the ckt operation, assume

$V_{cc} = +10V$

$V_{EE} = -10V$

$R_E = 4.7K\Omega$

$R_C = 6.8K\Omega$

and all transistors have $V_{BE} = 0.7V$

$$\therefore I_{E_1} + I_{E_2} = \frac{V_{EE} - V_{BE}}{R_E} = 1.978mA \approx 2mA.$$

$I_{E_1} \approx 1mA$

$I_{E_2} \approx 1mA$

We know that, $I_E = I_C + I_B$

as $I_B <<< I_C$

$\therefore I_E \approx I_C$

$\therefore I_{C_1} = 1mA$

$I_{C_2} = 1mA$

$\therefore V_o = V_{CC} - I_{C_2}R_C - V_{BE_3}$

$= 10 - (1mA \times 6.8K) - 0.7$

$= 2.5\ V.$

Case-2 ⇒

→ When positive voltage is applied at the INV terminal, the emitter voltage of Q_2 increases with non-inv terminal grounded.

→ It increases V_{BE_2} and hence I_{E_2} and I_{C_2} increases.

→ let, I_{C_2} increases from 1mA to 1.2 mA.

$\therefore V_o = V_{CC} - I_{C_2}R_C - V_{BE_3}$

$= 10 - (1.2mA \times 6.8K) - 0.7$

$= 1.14\ V.$

Case-3 ⇒

→ When positive voltage is applied to NON-INV. terminal with INV terminal grounded which increases emitter vtg of Q_1.

→ Since both emitter Q_1 and Q_2 are connected together, Q_2 also increases by same amount.

→ Since base of Q_2 is grounded. V_{BE_2} decreases which decreases I_{E_2} and I_{C_2}.

→ Therefore let I_{C_2} decreases from 1 mA to 0.8 mA

$$\therefore V_o = V_{CC} - I_{C_2} R_C - V_{BE}$$
$$= 10 - (0.8\,mA \times 6.8\,k\Omega) - 0.7$$
$$= 3.86\ V.$$

SUMMARY

(1).	Gnd	Gnd	$I_{C_2} = 1\,mA$	$V_o = 2.5\,V$	
(2).	Gnd	Vtg	$I_{C_2} = 1.2\,mA$	$V_o = 1.14\,V$	INV.
(3).	Vtg	Gnd	$I_{C_2} = 0.8\,mA$	$V_o = 3.86\,V$	NON INV.

***

Q2. Define the following terms as applied to an op-amp and mention their typical values for IC 741.

(i). CMRR.

(ii). PSRR.

(iii). Slew rate.

(iv) Input offset voltage.

(v). Input voltage range.

⇒ (1). CMRR ⇒

→ The ability of the op-amp in rejecting common mode inputs is defined as common mode rejection ratio (CMRR).

→ CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain 'A_{cm}'

$$CMRR = \frac{M}{A_{cm}}$$

→ The CMRR is usually expressed in decibels.

$$(CMRR)_{dB} = 20 \log_{10}\left(\frac{M}{A_{cm}}\right) dB.$$

→ Typical value = 90 dB.

(2). PSRR ⇒

→ The PSRR is the ability of the op-amp to reject variations in the power supply voltages.

$$PSRR = \frac{V_o\,(ripple)}{V_s\,(ripple)}$$

→ If a variation of 1 V in V_{CC} or V_{EE} causes the o/p to change by 1 V, then PSRR is 1 per volt.

→ Typical value = 30 $\mu V/V$

→ The PSRR is the ability of the op-amp to reject variations in the power supply voltages.

(3). Slew rate ⇒

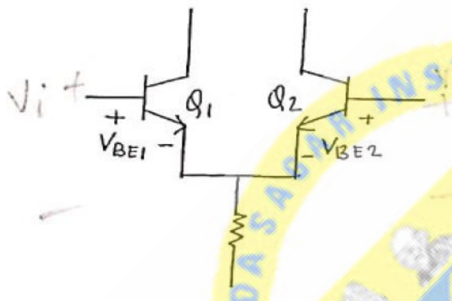
→ The slew rate 'S' of an op-amp is the ma
rate at which the o/p voltage can change.

→ When the slew rate is too slow for the I/
, then o/p will distort.

$$\text{Slew rate} = \frac{\Delta V}{\Delta t} \quad \text{or} \quad S = \left.\frac{dV_o}{dt}\right|_{max}$$

→ Typical value: 0.5 V/µsec.

(4). Input offset voltage ⇒



→ Suppose that the transistors are not perfectl
matched & that $V_{BE1} = 0.7V$ & $V_{BE2} = 0.6V$

→ With the i/p $V_i = 0$,

$$V_o = V_i - V_{BE1} + V_{BE2}$$
$$= 0 - 0.7V + 0.6V$$
$$= -0.1V$$

→ To set V_o to ground level, the i/p would have to
raised to +0.1 V. This is termed as input offset
voltage (V_{ios}).

→ Typical value: 1mV & Max^m value = 5mV.

(5). Input voltage range ⇒

→ The maximum effective positive-going and negative-going voltage that may be applied to the input of an op-amp is termed as its input voltage range.

→ Typical value : ±13 V when using a ±15 V supply.

Q.3. With a neat circuit diagram, explain direct coupled voltage follower with relavant design steps.

⇒

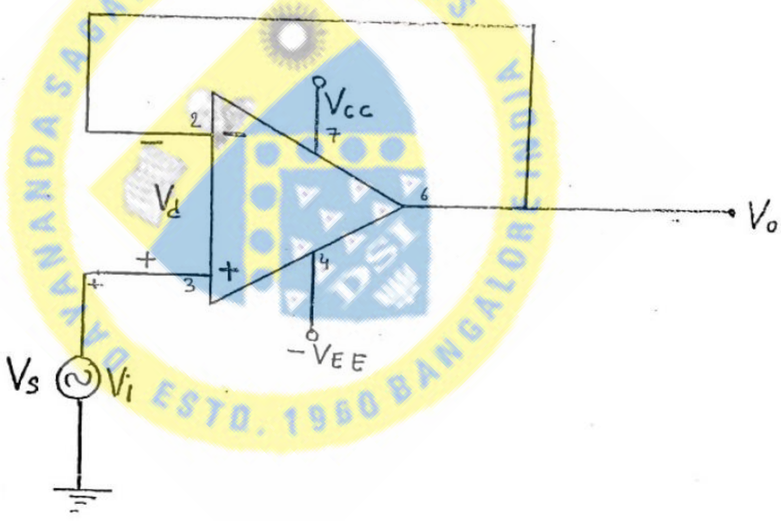


Fig: Directly coupled voltage follower.

→ Without using any external component, it is possible to use op-amp as a direct coupled voltage follower as shown.

→ Due to very high open loop gain (M) of the op-amp, there will be a very-very small difference b/w the input vtg 'V_i' & the o/p voltage V_o.

→ The differential I/p should be such as to produce a o/p close to V_i & is given by:

$$V_d = \frac{V_i}{M}$$

where, M → open loop gain of op-amp.

→ Applying KVL from i/p to o/p:

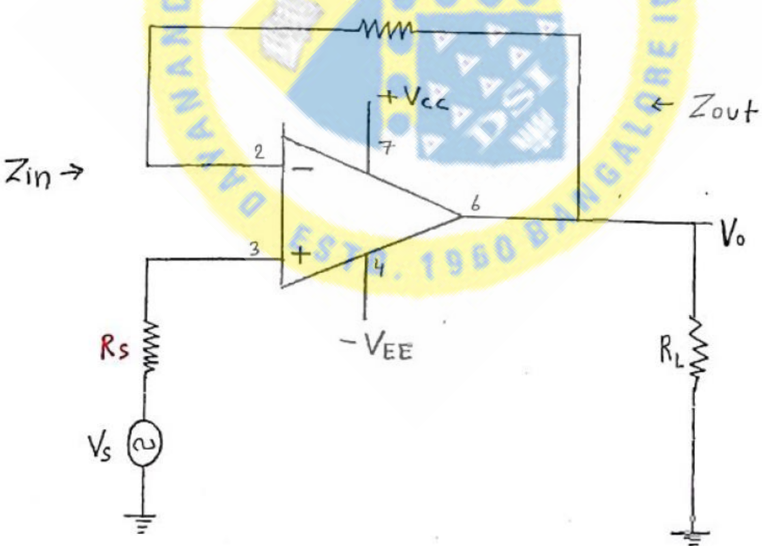
$$V_i - V_d - V_o = 0$$

$$\Rightarrow V_o = V_i - V_d$$

$$V_o = V_i - \frac{V_i}{M}$$

$$\Rightarrow V_o = V_i\left[1 - \frac{1}{M}\right]$$

→



→ In directly coupled voltage follower, the resistor R_1 is used between o/p & inverting terminal to match the source resistance R_s.

→ The i/p impedance of voltage follower is given by:

$$\boxed{Z_{in} = (1+M)Z_i} \quad \text{as } \beta = 1$$

→ The o/p impedance of V.F is given by

$$\boxed{Z_{out} = \frac{Z_o}{(1+M)}} \quad \ldots \text{as } \beta = 1.$$

→ load vtg (V_L) is given by:

$$V_L = I_L R_L$$

$$= \frac{V_o}{Z_{out} + R_L} \times R_L$$

As $Z_{out} <<< R_L$

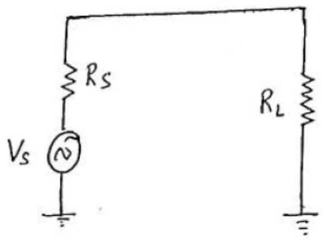
$$= \frac{V_o}{R_L} \times R_L$$

$$\boxed{V_L = V_o}$$

Thus there is effectively no signal loss, and all of the output voltage V_o appeared across load resistance R_L

Case - II

Consider load resistance R_L is directly connected to source as shown.



$$I = \frac{V_s}{R_s + R_L}$$

$$V_L = I R_L = \frac{V_s}{R_s + R_L} \times R_L.$$

Thus some part of V_s gets lost (due to R_s), when load is directly connected.

Q.4 With a neat diagram explain dire coupled Non-inverting amp^r with releva design steps.

⇒

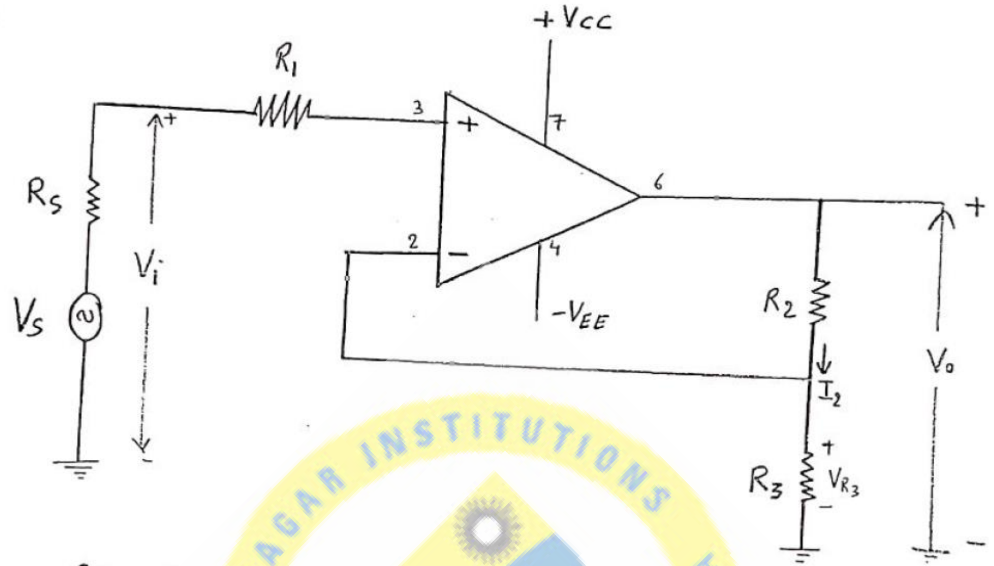


Fig. Directly coupled NON-INV ampr.

⇒ The voltage gain of NON-INV amplifier is :

$$\boxed{A_V = \frac{R_2 + R_3}{R_3}}$$

Design steps:

(1). The potential divider resistor values are determined by using V_i, V_o, and I_2.

$$R_3 = \frac{V_{R_3}}{I_2}$$

but $V_{R_3} = V_i$

$$\Rightarrow \boxed{R_3 = \frac{V_i}{I_2}}$$

→ The o/p voltage 'V_o' appears across $(R_2 + R_3)$.
Applying KVL to o/p circuit:

$$V_o - I_2 R_2 - I_2 R_3 = 0$$

$$\Rightarrow (R_2 + R_3) I_2 = V_o$$

$$\Rightarrow (R_2 + R_3) = \frac{V_o}{I_2}$$

$$\Rightarrow \boxed{R_2 = \frac{V_o}{I_2} - R_3}$$

(2). To equalize the $I_B R$ voltage drop at the op-amp I/p's, R1 is calculated as:

$$\boxed{R_1 = (R_2 \,||\, R_3)}$$

(3). If R1 as determined from above equ^n is not very much larger than the source resistance i.e. $R_1 << R_3$. then,

$$\boxed{(R_S + R_1) = (R_2 \,||\, R_3)}$$

Q.5 With a neat circuit diagram, explain direct coupled Inverting amplifier with relevant design steps.

→ The o/p voltage 'V_o' appears across (R_2+R_3).
Applying KVL to o/p circuit:

$$V_o - I_2R_2 - I_2R_3 = 0$$

$$\Rightarrow (R_2+R_3)\,I_2 = V_o$$

$$\Rightarrow (R_2+R_3) = \frac{V_o}{I_2}$$

$$\Rightarrow \boxed{R_2 = \frac{V_o}{I_2} - R_3}$$

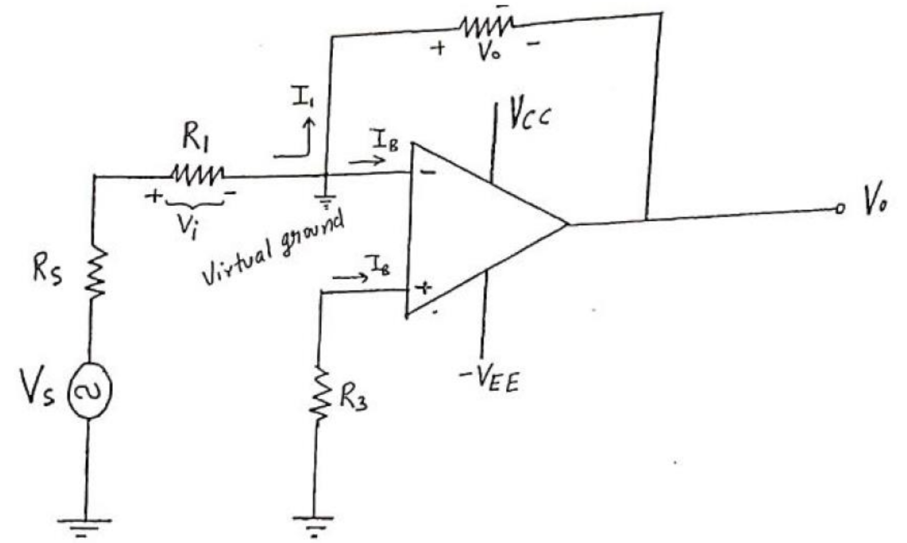
(2). To equalize the I_BR voltage drop at the op-amp I/P's, R1 is calculated as:

$$\boxed{R_1 = (R_2 \,||\, R_3)}$$

(3). If R1 as determined from above equ^n is not very much larger than the source resistance i.e. $R_1 << R_3$. then,

$$\boxed{(R_S + R_1) = (R_2 \,||\, R_3)}$$

Q.5 With a neat circuit diagram, explain direct coupled Inverting amplifier with relevant design steps.



→ The gain of the INV- ampr is given by

$$A_v = -\frac{R_2}{R_1}$$

Design steps ⇒ "For 741".

(1). Current I_1 is to be selected much higher than $I_{B(max)}$ of the op-amp.

$$I_1 = 100 \times I_{B\,max}$$

(2). $$R_1 = \frac{V_i}{I_1}$$

(3). $$R_2 = \frac{V_o}{I_1}$$

(4). When looking out from each I/p terminal of op-amp

$$R_3 = R_1 \| R_2$$

And if R_1 is not very much larger than the source resistance, then

$$R_3 \approx (R_1 + R_S) \| R_2$$

For LF353 ⇒

(i). $R_2 = 1\,M\Omega$

(ii). $A_V = \frac{R_2}{R_1} \Rightarrow R_1 = \frac{R_2}{A_V}$

(iii). $R_3 \approx (R_1 \| R_2)$

Q.6. Explain direct coupled 2-I/p non-inverting summing amp^r with neat diagram and necessary design steps:

⇒

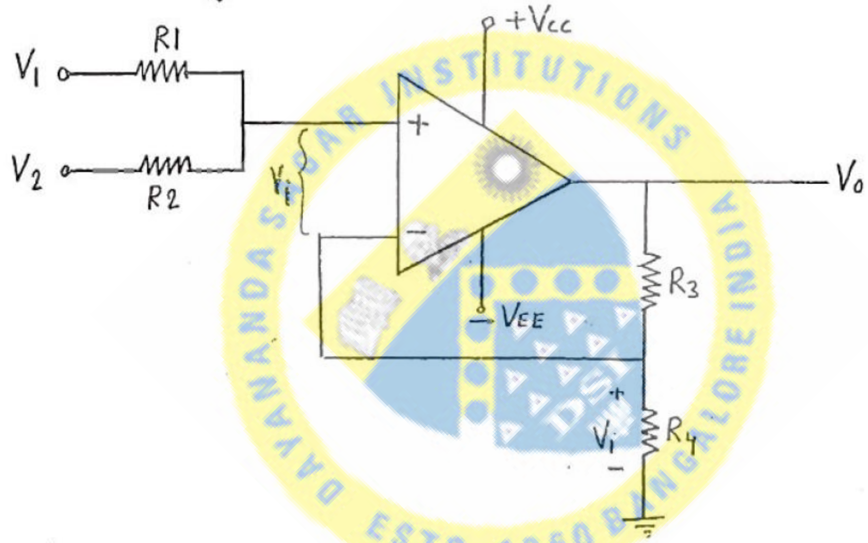


Fig 2 I/p NON-INV summing amp^r.

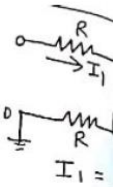
→ Fig shows a non-inv. summing amp^r. The output will be a direct sum of (+ve) i/p signals.

→ The equation for the o/p vtg can be derived by using superposition theorem.

→ Case I: let $V_2 = 0$ &

$R_1 = R_2 = R$.

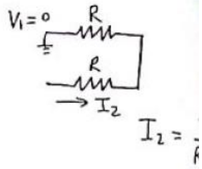
$$V_{i_1} = I_1 R_1 = \frac{V_1}{R+R} \cdot R = \frac{V_1 R}{2R} = \frac{V_1}{2} \quad \text{—— (1)}$$



Case - II

Let, $V_1 = 0$ & $R_1 = R_2 = R$.

$$V_{i_2} = I_2 R = \frac{V_2 R}{R+R} = \frac{V_2 R}{2R} = \frac{V_2}{R} \quad \text{—— (2)}$$



→ The i/p voltage V_i is given by:

$$V_i = V_{i_1} + V_{i_2}$$
$$= \frac{V_1}{2} + \frac{V_2}{2}$$
$$= \frac{V_1 + V_2}{2}$$

→ For Non-inverting ampr, the voltage gain is given by : $A_V = \frac{R_3 + R_4}{R_4}$

→ WKT $A_V = \frac{V_o}{V_i}$

$$\Rightarrow V_o = A_V \cdot V_i$$
$$= \left(\frac{R_3 + R_4}{R_4}\right)\left(\frac{V_1 + V_2}{2}\right)$$

If $R_3 = R_4 = R$

$$= \left(\frac{2R}{R}\right)\left(\frac{V_1 + V_2}{2}\right)$$

$$\Rightarrow \boxed{V_o = (V_1 + V_2)}$$

Q.7 Sketch an op-amp Difference amplifier circuit. Explain the operation of the circuit and derive an equation for an output voltage.

⇒→ A difference amplifier or differential amplifier, amplifies the difference between the two i/p signals.

→ Since the open-loop gain of the op-amp is very large, it has to be used with negative feedback.

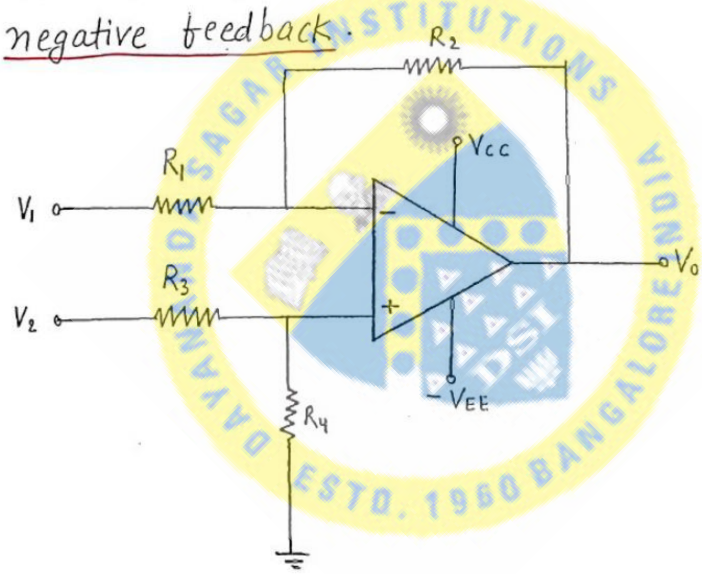


Fig. Difference ampr ckt.

Operation:

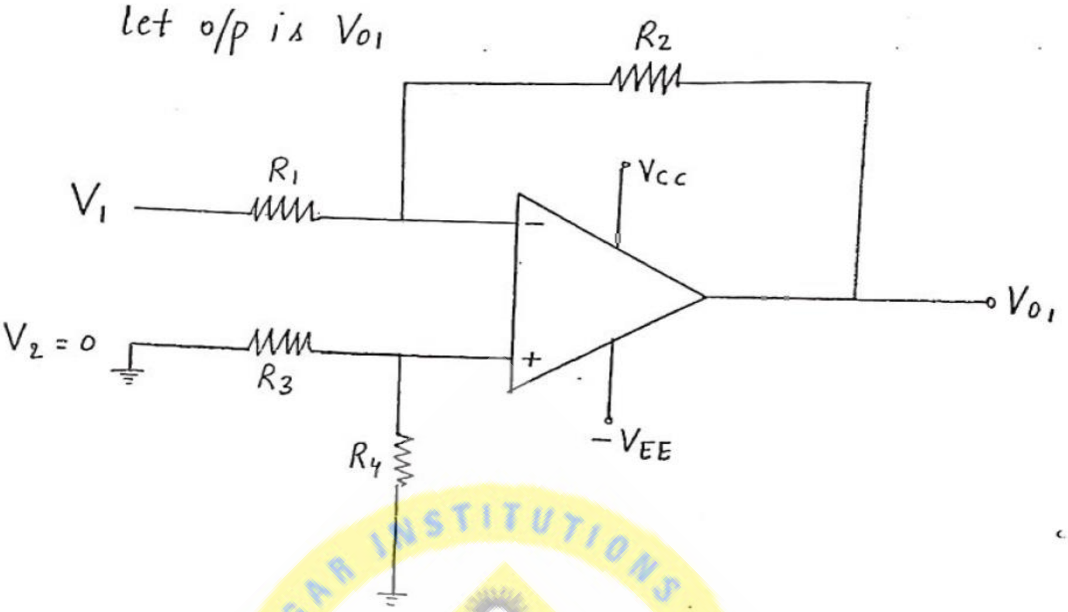
→ Let us use superposition principle to find out the expression for the o/p.

Case-I :

V_1 acting

$V_2 = 0V$ (grounded)

let o/p is V_{o1}



→ Now the fig. acts as an INV ampr.

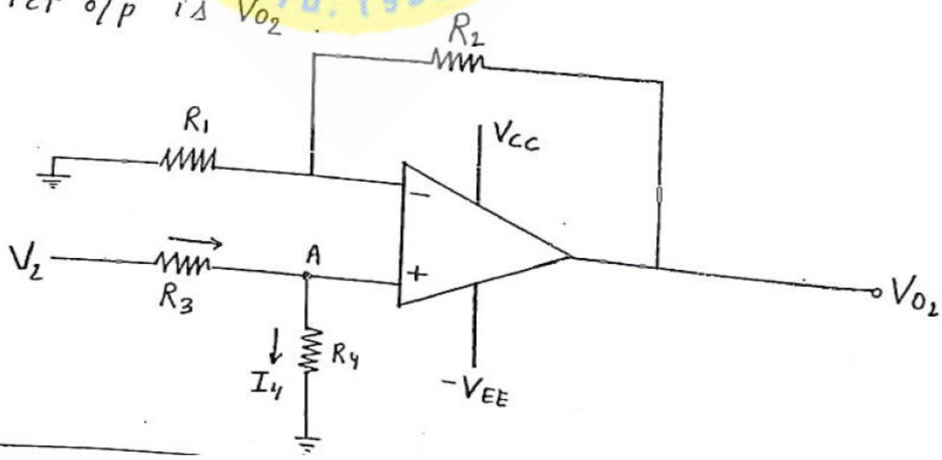
$$\boxed{V_{o1} = -\frac{R_2}{R_1} \cdot V_1} \quad (1)$$

Case-II :

V_2 acting

$V_1 = 0V$ (grounded)

let o/p is V_{o2}



→ Now it acts as NON-INV ampr and hence

$$V_{o_2} = A_v \cdot V_A$$

WKT, the gain of the NON-INV ampr is given by. $A_v = \left(1 + \frac{R_2}{R_1}\right)$

$$\therefore \boxed{V_{o_2} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_A} \quad \text{—— (2)}$$

→ From above figure, voltage at A is given by:

$$V_A = I \cdot R_4$$

where,

$$I = \frac{V_2}{R_3 + R_4}$$

$$\therefore \boxed{V_A = V_2 \cdot \frac{R_4}{R_3 + R_4}} \quad \text{—— (3)}$$

→ Substituting (3) in (2), we get

$$\boxed{V_{o_2} = \left(1 + \frac{R_2}{R_1}\right)\left(V_2 \cdot \frac{R_4}{R_3 + R_4}\right)} \quad \text{—— (4)}$$

→ By the principle of superposition:

$$V_o = V_{o_1} + V_{o_2}$$

$$= -\frac{R_2}{R_1} \cdot V_1 + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) \cdot V_2$$

Select $R_3 = R_1$, $R_4 = R_2$

$$= -\frac{R_2}{R_1} V_1 + \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_2$$

$$= -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2$$

$$V_o = \frac{R_2}{R_1}[V_2 - V_1]$$

When, $R_1 = R_2$

$$\boxed{V_o = (V_2 - V_1)}$$

→ Now the o/p is the direct difference of the two i/p vtg.

Q8. Define with typical value:

(i). CMRR
(ii). PSRR
(iii) Slew rate.
(iv) i/p offset vtg.
(v). o/p offset vtg.

⇒ (V). o/p offset vtg ⇒

→ For the o/p vtg to be exactly equal to the i/p, the transistor Q_1 & Q_2 must be perfectly matched.

→ The o/p can be calculated as:

$$V_i - V_{BE1} + V_{BE2} - V_o = 0$$

$$\Rightarrow \boxed{V_o = V_i - V_{BE_1} + V_{BE2}}$$

With, $V_{BE1} = V_{BE2}$ and $V_i = 0$

o/p ⇒ $\boxed{V_o = V_i = 0}$.

$$V_o = \frac{R_2}{R_1}[V_2 - V_1]$$

When, $R_1 = R_2$

$$\boxed{V_o = (V_2 - V_1)}$$

→ Now the o/p is the direct difference of the two i/p vtg.

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With, $V_{BE1} = V_{BE2}$

and $V_i = 0$

o/p ⇒ $\boxed{V_o = V_i = 0}$.

Numericals:

Q.1. Design an INV ampr using 741 op-amp. The vtg gain is to be 50 and the voltage amplitude is to be 2.5V.

⇒ $I_2 = 100\, I_{B_{max}} = 100 \times 500\, nA = 50\, \mu A$

$V_i = \dfrac{V_o}{A_{CL}} = \dfrac{2.5V}{50} = 50\, mV$

$R_1 = \dfrac{V_i}{I_i} = \dfrac{V_i}{I_2} = \dfrac{50\, mV}{50\, \mu A} = 1\, K\Omega$.

$R_2 = \dfrac{V_o}{I_i} = \dfrac{V_o}{I_2} = \dfrac{2.5V}{50\, \mu A} = 50\, K\Omega$.

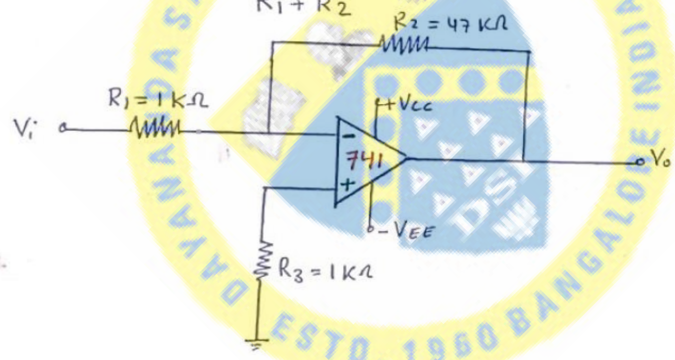
$R_3 = R_1 \| R_2 = \dfrac{R_1 . R_2}{R_1 + R_2} = 979.59\, \Omega$

Standard value:

$R_1 = 1 K\Omega$

$R_2 = 47 K\Omega$

$R_3 = 1 K\Omega$



By using LF353 ⇒

Select, $R_2 = 1 M\Omega$.

$R_1 = \dfrac{R_2}{A_{CL}} = \dfrac{1 M\Omega}{50} = 20\, K\Omega$

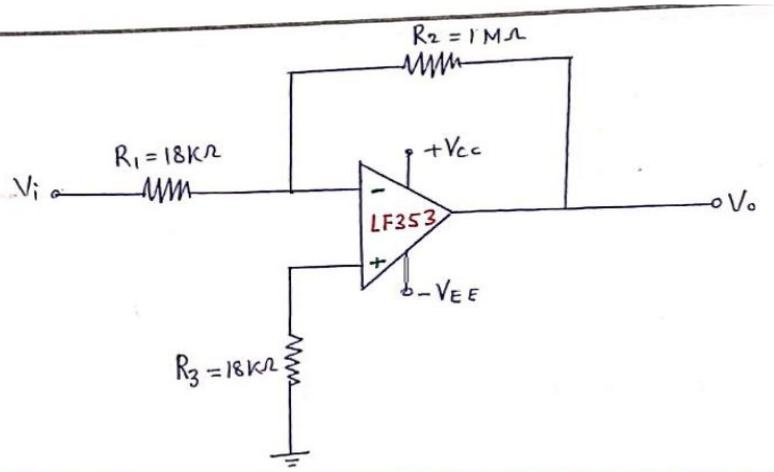
Standard value:

$R_1 = 18\, K\Omega$.

$R_3 = R_1 \| R_2 = 1 M\Omega \| 20 K\Omega$

$= 19.607\, K\Omega$.

$R_3 = 18\, K\Omega$.



Q.2. A NON-INV ampr is to amplify a 100 mV signal to a level of 3V, using 741 op-amp. Design a suitable circuit. (consider $I_{Bmax} = 500n$, $R_s = 1K\Omega$)

$\Rightarrow \quad I_2 = 100\, I_{Bmax} = 100 \times 500\,nA = 50\,\mu A$

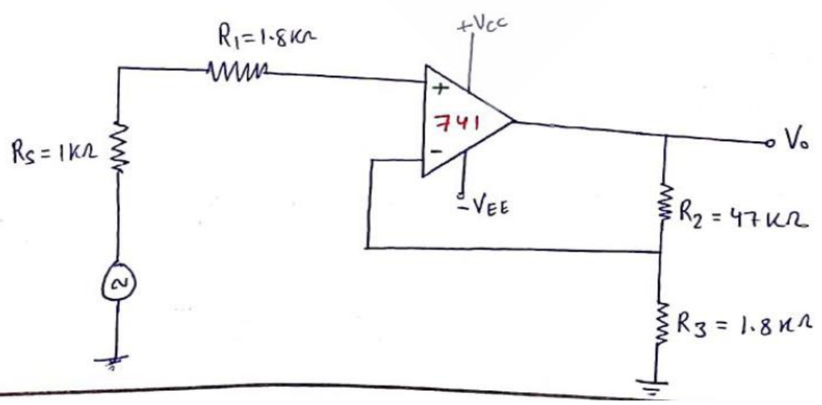
$R_3 = \frac{V_i}{I_2} = \frac{100\,mV}{50\,\mu A} = 2\,K\Omega$ — Standard value: $R_3 = 1.8\,K\Omega$.

Now, $I_2' = \frac{V_i}{R_3} = \frac{100\,mV}{1.8\,K\Omega} = 55.6\,\mu A$

$R_2 = \frac{V_o}{I_2'} - R_3 = \frac{3V}{56\mu A} - 1.8K\Omega = 58\,K\Omega$, $R_2 = 47\,K\Omega$.

$R_1 = R_2 \| R_3 = 1.8K\Omega \| 47K\Omega = 1.733\,K\Omega$ $R_1 = 1.8\,K\Omega$

$R_s = 1\,K\Omega$.



By-using LF353 →

$$A_v = \frac{V_o}{V_i} = \frac{3V}{0.1V} = 30.$$

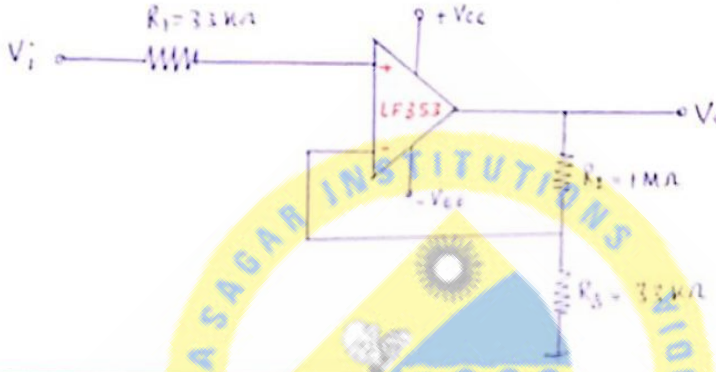
Now Choose $\boxed{R_2 = 1\,M\Omega}$

$$R_3 = \frac{R_2}{A_v - 1} = \frac{1M\Omega}{30-1} = 34.48\,K\Omega$$

Standard value $\boxed{R_3 = 33\,K\Omega}$.

$$R_1 = R_2 \,||\, R_3 = 1M\Omega \,||\, 33\,K\Omega = 31.9\,K\Omega$$

$\boxed{R_1 = 33\,K\Omega}$.



Q.3. A NON-INV amp is to amplify a 100 mV signal to a level of 5V, using a 741 op-amp design a suitable ckt.

$R_1 = 1.8\,K\Omega$

$R_2 = 82\,K\Omega$.

$R_3 = 1.8\,K\Omega$

$R_5 = 1\,K\Omega$.

Q.4. Design a DC NON-INV amp to amplify 100 mV signal using 741 op-amp to a level of 4V.

$R_1 = 1.8\,K\Omega$

$R_2 = 68\,K\Omega$.

$R_3 = 1.8\,K\Omega$

$R_4 = 1\,K\Omega$.

Q.3. The NON-INV amp^r uses MA 741 op-amp with $R_1 = R_3 = 2.2\,K\Omega$ and $R_2 = 220\,K\Omega$. Determine maximum possible output offset vtg due to:

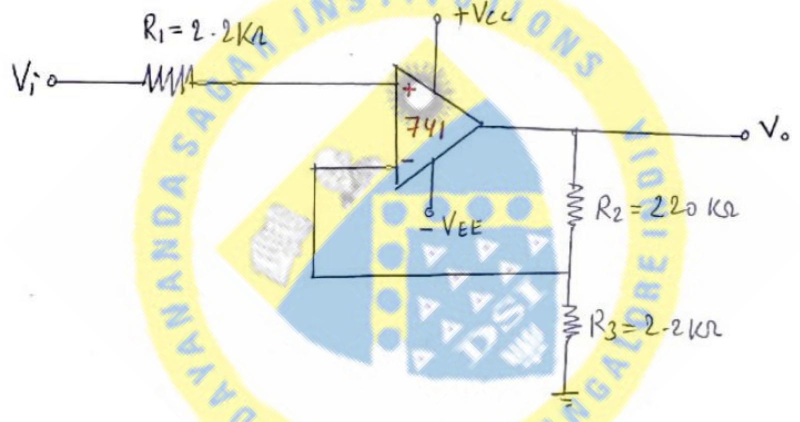
(i) input offset vtg of 5 mV.

(ii) input bias current of $I_{B\,max} = 500\,nA$

(iii) input offset current of $I_{ios} = 200\,nA$

(iv) resistance tolerance of $\pm 10\%$.

⇒



(i). $V_{i_{os}} = 5\,mV$.

For Non-inv amp^r ⇒ $A_{CL} = 1 + \frac{R_2}{R_3} = 1 + \frac{220\,K\Omega}{2.2\,K\Omega} = 101$.

$V_{o(os)i} = A_{CL} \times V_{i_{os}} = 101 \times 5\,mV$ ⇒ $\boxed{V_{o(os)i} = 505\,mV}$

(ii). $I_B = 500\,nA$

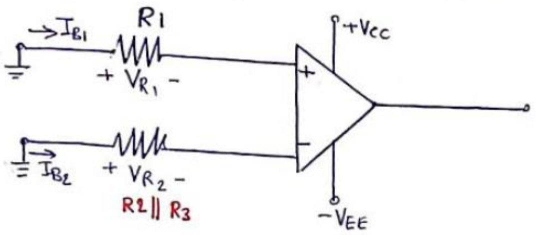
$R_2 || R_3 = 220\,K\Omega \,||\, 2.2\,K\Omega = 1.98\,K\Omega$.

Input resistance difference:

$R = R_1 - (R_2 || R_3) = 2.2\,K\Omega - 1.98\,K\Omega = 220\,\Omega$.

$V_{ios} = I_B \times R = 500\,nA \times 220\,\Omega = 110\,\mu V$.

$V_{o(os)2} = A_{CL} \cdot V_{ios} = 101 \times 110 \mu V = 11.1 \, mV$



Input bias current flow through R_1 & $(R_2 || R_3)$

(iii). $I_{ios} = 200 \, nA$.

$V_{ios} = I_{ios} \times R_1 = 200 \, nA \times 2.2 \, K\Omega = 440 \, \mu V$.

$V_{o(os)3} = A_{CL} \cdot V_{ios} = 101 \times 440 \mu V = 44.4 \, mV$.

(iv). $R_1 = 2.2 \, K\Omega + 10\% = 2.42 \, K\Omega$

$R_2 || R_3 = 1.98 \, \Omega - 10\% = 1.78 \, K\Omega$

$V_{ios} = I_B (R_1 - R_2 || R_3) = 500 \, nA \, (2.42 \, K\Omega - 1.78 \, K\Omega) = 320 \mu V$

$V_{o(os)4} = A_{CL} \cdot V_{ios} = 101 \times 320 \, \mu V = 32.3 \, mV$.

Ans. Due to all errors maximum output offset voltage is:

$V_{o(os)max} = V_{o(os)1} + V_{o(os)2} + V_{o(os)3} + V_{o(os)4}$

$= 505 \, mV + 11.1 \, mV + 44.4 \, mV + 32.3 \, mV$

$= 593 \, mV$.

(i). $V_{o1} = 505 \, mV$
(ii) $V_{o2} = 11.1 \, mV$
(iii) $V_{o3} = 44.4 \, mV$
(iv) $V_{o4} = 32.3 \, mV$
$V_{omax} = 593 \, mV$