LIC

Unit - I

Op-Amp Fundamentals

Ic's are classified according to no. of components integrated on the same chip.

SSI → Small Scale Integration
⇒ less than about 10 gates are fabricated on a chip.

MSI → Medium Scale Integration
⇒ has more than 10 gates but less than 100 gates per chip.

LSI → Large Scale Integration
⇒ has more than 100 gates but less than 1000 gates per chip.

VLSI → Very large Scale Integration
⇒ has more than 10,000 components per chip.

All the components of each circuit are fabricated on a single silicon chip is known as Integrated circuits (IC's).

There are two types of Ic's
(1) Digital Ic's (2) Linear Ic's

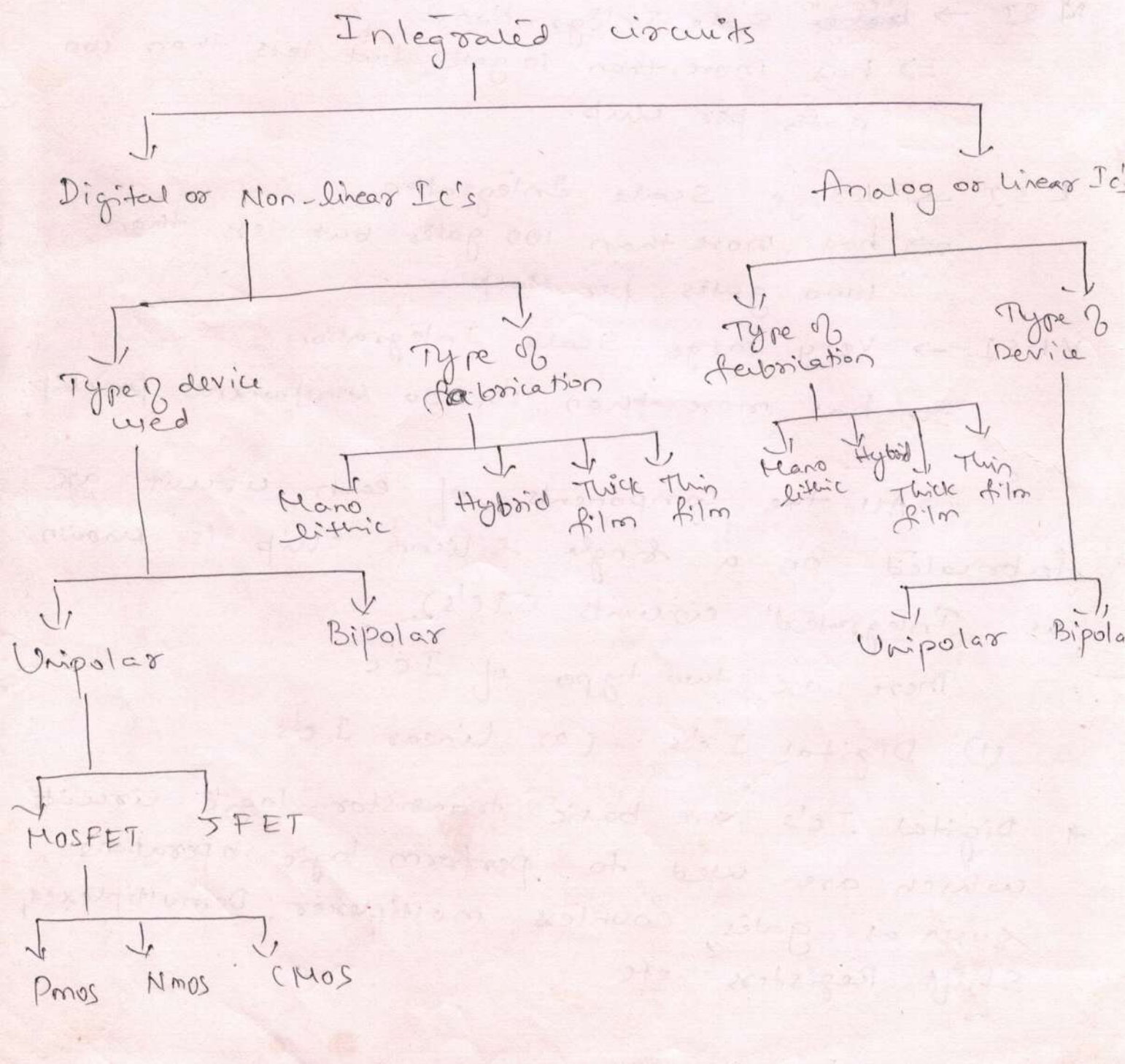
* Digital Ic's are basic transistor logic circuits which are used to perform logic operations such as gates, counters, multiplexer, Demultiplexer, Shift Registers etc

Digital Ic's are concerned with only two level of voltage a high and low.

Ex:- Nand gate, counters, shift Registers etc

* Linear Ic's are equivalent transistor networks, such as amplifiers, filters, frequency multipliers,

Ex:- op amps.

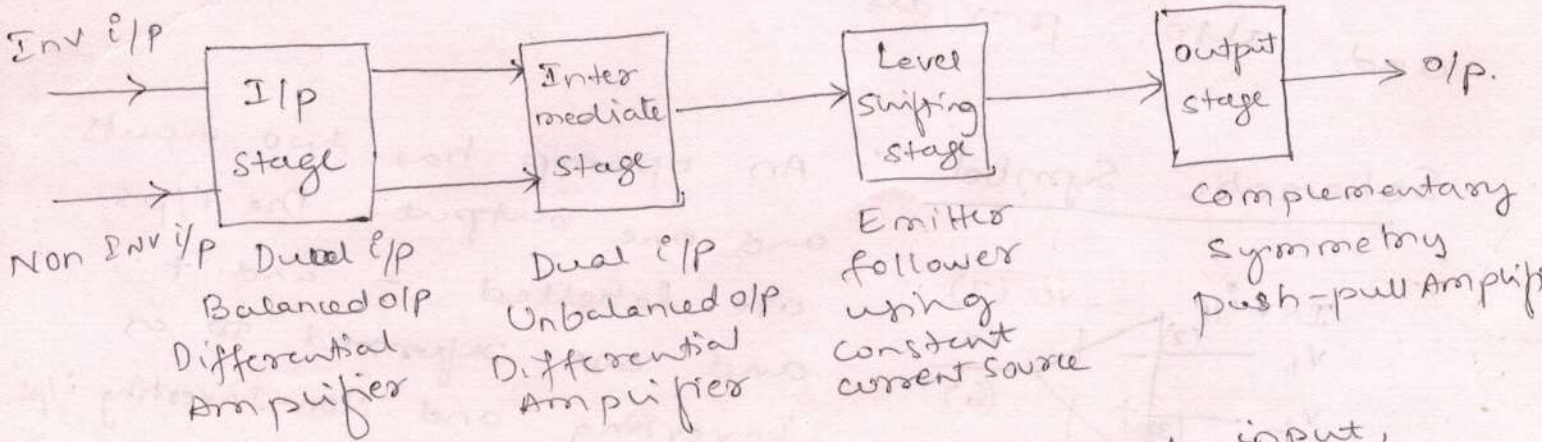


Operational Amplifier (op-amp)

An operational amplifier is a Direct Coupled high gain Amplifier with two high input-impedence terminals and one low-impedence output terminal.

It finds its use in performing mathematical operations such as addition, subtraction, multiplication, integration and Differentiation. other than these mathematical operations op-Amp can also be used to amplify ac and dc signal, used as a filter, oscillator, comparator, regulator etc.

Block diagram of an op-Amp



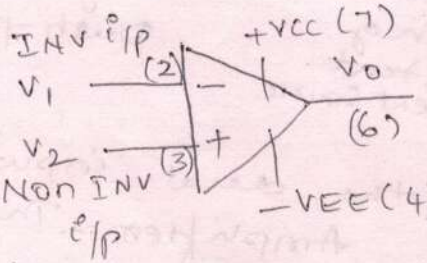
The i/p stage is the dual input, balanced output Differential Amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes i/p resistance of the op-Amp.

The intermediate stage is usually another differential amplifier which is driven by the output of the first stage. In most of the amplifier intermediate stage is dual i/p, unbalanced output. Because direct coupling is used, the dc voltage at the output of the intermediate stage is well above ground potential.

Therefore the level translator circuit is used after the intermediate stage to shift the dc level at the output of intermediate stage downward to zero volts.

Usually the output stage is complementary symmetry push-pull amplifier. The output stage increases the output voltage swing and raises the current supplying capability of the op-Amp and also provides low output resistance.

Schematic Symbol : An opamp has two inputs and one output. The i/ps are labelled − and +. and are referred to as Inverting and Non-Inverting i/ps



An AC or DC signal applied to the non-inverting i/p produces an output which is in phase with the input. Ily an AC or DC signal applied to the inverting input produces an output which is out-of phase with the i/p signal.

* Basic operational Amplifier circuit

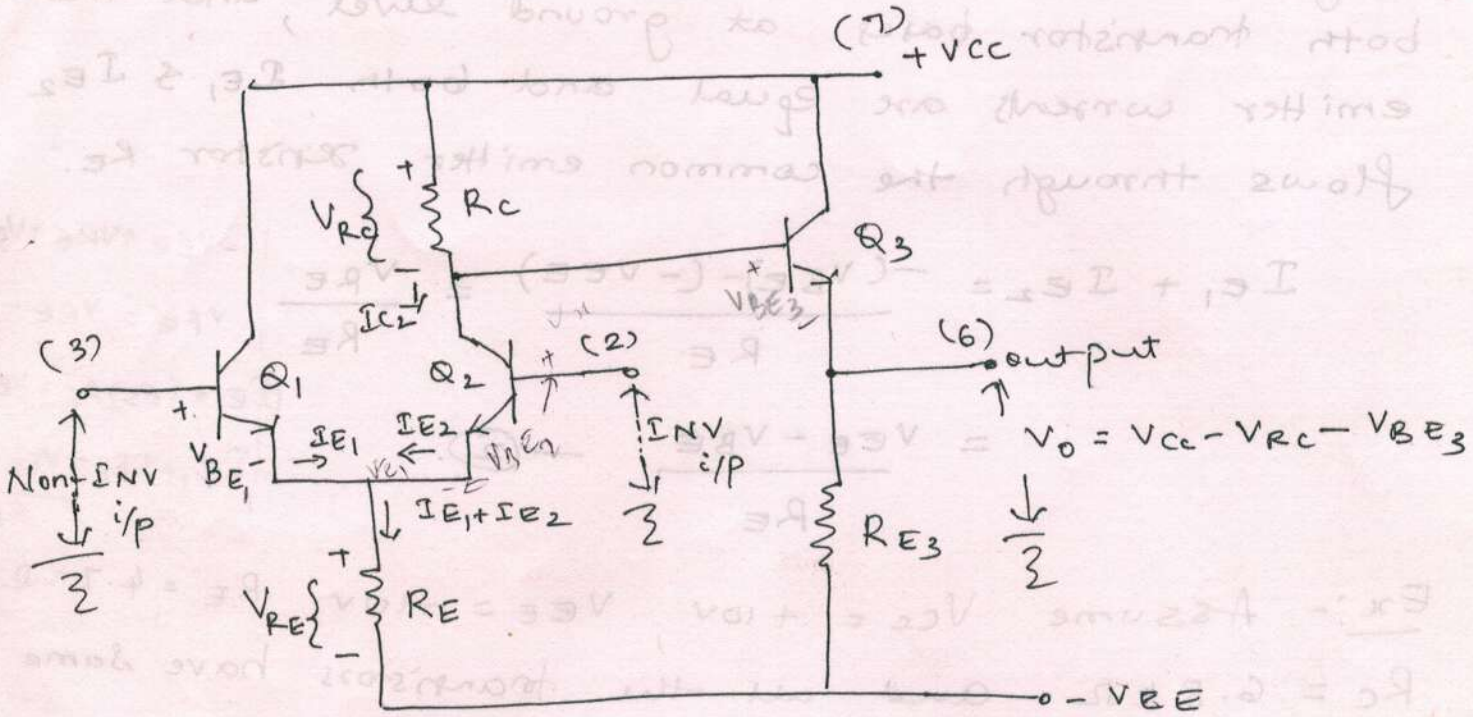


fig (1) Basic circuit of (4) OP AMP

The basic circuit of an op-Amp is shown in fig(1). It is provided with plus and minus supply voltages (+Vcc and -VEE). It has two input terminals known as inverting and non-inverting inputs. Transistors Q_1 and Q_2 forms a difference amplifier. when a difference input voltage is applied to the bases of Q_1 and Q_2 it produces a voltage change at the collector of Q_2. Transistor Q_3 acts as an emitter follower which provides a low output impedence. In fig (1) the two input terminals are grounded.

The D.C. output voltage at pin 6 is

$$V_o = V_{cc} - V_{RC} - V_{BE_3}$$

$$V_{RC} = I_{C_2} R_c$$

$$\therefore V_o = V_{cc} - I_{C_2} R_c - V_{BE_3} \quad \text{—} (1)$$

Assuming Q_1 and Q_2 are matched transistor ie may have same V_{BE} and current gain with both transistor bases at ground level, and the emitter currents are equal and both I_{E_1} & I_{E_2} flows through the common emitter resistor R_E.

$$I_{E_1} + I_{E_2} = \frac{-(V_{BE}) - (-V_{EE})}{R_E} = \frac{V_{RE}}{R_E}$$

$-V_{EE} + V_{RE} + V_{BE}$

$V_{RE} = V_{EE} - V_{BE}$

$(I_{E_1} + I_{E_2}) R_E = V_{EE}$

$$\therefore I_{E_1} + I_{E_2} = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{V_{EE} - V_{BE}}{R_E} \quad -(2)$$

Ex:- Assume $V_{CC} = +10V$, $V_{EE} = -10V$, $R_E = 4.7 k\Omega$, $R_C = 6.8 k\Omega$ and all the transistors have same $V_{BE} = +0.7V$.

From eq(2), $I_{E_1} + I_{E_2} = \frac{V_{EE} - V_{BE}}{R_E} = \frac{10 - 0.7}{4.7 \times 10^3}$

$$= 2 mA$$

$\therefore I_{E_1} = I_{E_2} = 1mA.$

$I_{C_2} \simeq I_{E_2} = 1mA.$

From eqn (1),

$$V_0 = V_{CC} - I_{C_2} R_C - V_{BE_3}$$

$$= 10 - 1 \times 10^{-3} \times 6.8 \times 10^3 - 0.7$$

$$V_0 = 2.5V$$

If a positive voltage is applied at the non-inverting input, base of Q_1 is pulled up by the input voltage. The emitter voltage of Q_1 also increases by the same amount since both emitters of Q_1 and Q_2 are connected together voltage at emitter of Q_2 also increases by the

same amount. Since base of Q_2 is grounded, V_{BE_2} decreases which decreases emitter current I_{E_2} of Q_2, so also I_{C_2}.

let I_{C_2} decreases by 0.2 mA ie from 1mA to 0.8 mA.

As $I_{E_1} I_{E_2}$
But
$V_{BE_2} + V_{RE} = V_E$
as V_{RE} V_{BE_2}
to maintain
VEE const

Then $V_O = V_{CC} - I_{C_2} R_C - V_{BE}$

$= 10 - 0.8 \times 10^{-3} \times 6.8 \times 10^3 - 0.7$

$V_O \cong 3.9\,V$

Since V_O changes from 2.5V to 3.9V when a positive voltage is applied at non-inverting terminal, which shows a positive voltage at NI terminal produces positive increase in voltage.

when a positive voltage is applied at the inverting input, emitter voltage of Q_2 increases with non-inverting input is grounded, this increa V_{BE_2} and hence I_{E_2} and I_{C_2}.

let I_{C_2} increases from 1mA to 1.2 mA, then

$V_O = V_{CC} - I_{C_2} R_C - V_{BE_3} = 10 - 1.2 \times 10^{-3} \times 6.8 \times 10^3 - 0.7$

$V_O \cong 1.1\,V$

This shows V_O decreases from 2.5V to 1.1V, a change of $-1.4\,V$. This shows a positive voltage at the inverting input produces a negative voltage change in the output.

The Basic op-amp circuit consists of a differential amplifier stage with two i/ps, inverting and non-inverting input. It has a voltage follower circuit (output stage).

The differential amplifier offers a high input impedance at both inputs and it produces a voltage gain. The output stage gives op-amp a low output impedance. A practical op-amp has more complex circuit than shown in fig(1)

Operational Amplifier Parameters

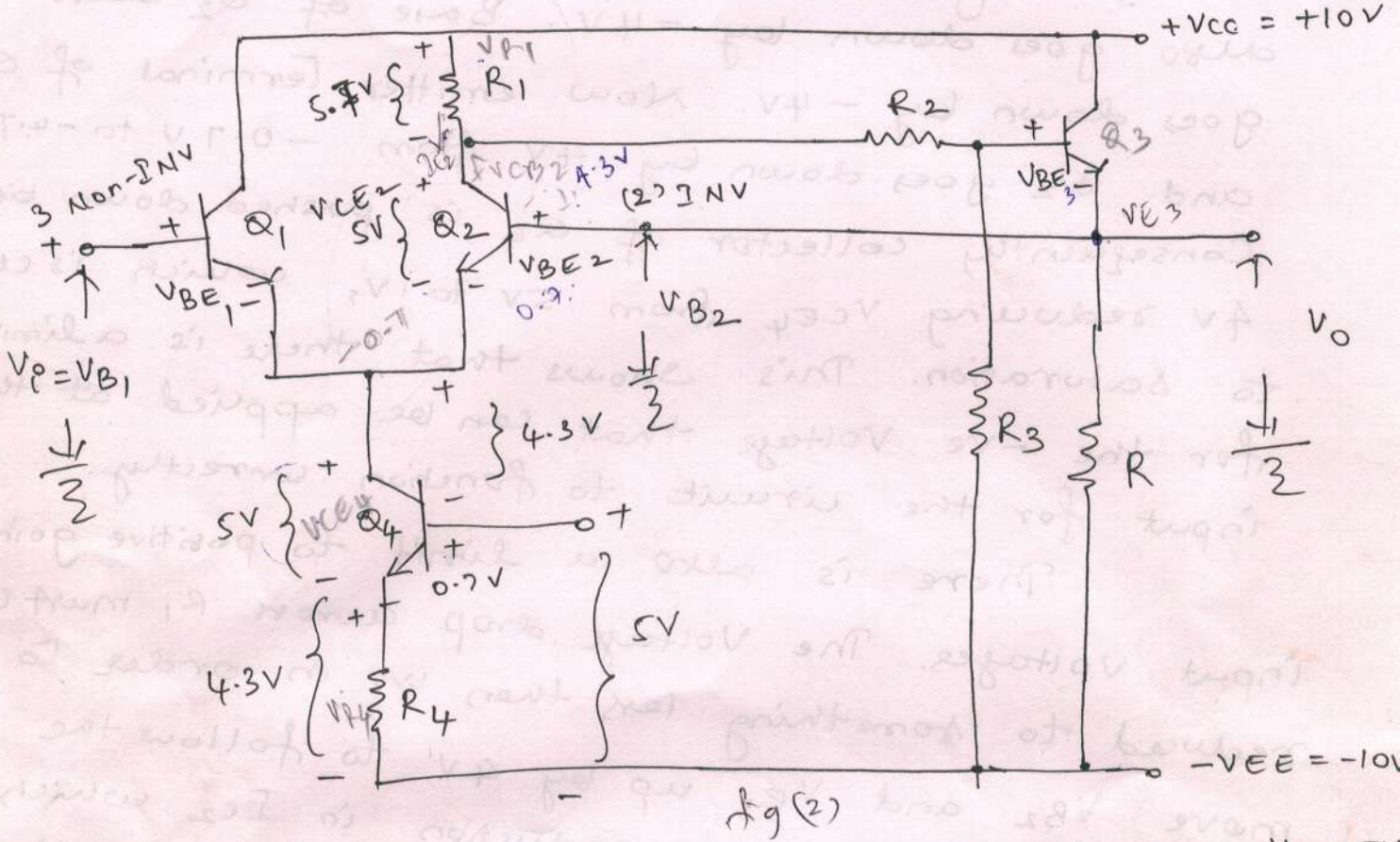
The performance of op-amp depends upon the type of op-amp used.

1. Each opamp has a maximum range of input and output voltage.
2. Due to bias voltages, suppy voltage variations and a.c ripple on suppy voltage, unwanted outputs can occur.
3. Due to mismatch of opamp input transistors and dc to input bias current, unwanted output voltage can be produced.
4. The input impedance of opamp is normally very high and output impedance of op-amp is normally very low, But with negative feedback Zin can be further increased and output impedance Zout can be forther decrease
5. There is a limit on how fast output voltage of opamp can be made to change and a limit on the highest signal freqeency that can be used.

Input and output Voltage

Input Voltage Range

The basic opamp circuit to function as a voltage follower is shown in fig(2).



fig(2)

The circuit might be designed to have $V_{CE}=5V$ across transistors Q_2 and Q_4. with a $\pm 10V$ supply and bases of Q_1 and Q_2 at ground level, the voltage drop across R_1 and R_4 would be 5.7V and 4.3V respectively.

$$-V_{BE_1} - V_{CE_4} - V_{R_4} + V_{EE} = 0$$
$$-0.7 - 5V - V_{R_4} + 10V = 0$$
$$\therefore V_{R_4} = 4.3V$$

$$V_{CB_2} + V_{R_1} = 10V$$
$$4.3 + V_{R_1} = 10V$$
$$V_{R_1} = 5.7V$$

$V_{CE_2} = 5V$, $V_{BE_2} = 0.7V$

$$V_{CB_2} + V_{R_1} - 10 = 0$$
$$V_{CE_2} + V_{BE_2} + V_{R_1} - 10 = 0$$
$$5 + 0.7 + V_{R_1} - 10 = 0$$
$$\Rightarrow V_{R_1} = 10 - 4.3$$

There is a limit for the range of input voltage variations as explained below.

If the input voltage at the base of Q_1 goes to $-4V$, being voltage follower, output voltage V_o also goes down by $-4V$. Base of Q_2 also goes down by $-4V$. Now emitter terminal of Q_1 and Q_2 goes down by 4V from $-0.7V$ to $-4.7V$. Consequently collector of Q_4 is pushed down by 4V reducing V_{CE_4} from 5V to 1V, which is close to saturation. This shows that there is a limit for the -ve voltage that can be applied at the input for the circuit to function correctly.

There is also a limit to positive going input voltages. The voltage drop across R_1 must be reduced to something less than 1V. In order to move V_{B_2} and V_{E_3} up by 4V to follow the i/p. This requires a reduction in I_{C_2} which makes Q_2 to approach cutoff. Hence the i/p voltage cannot be allowed to become large enough to drive Q_2 to cutoff.

This shows that there is a limit for the input voltage range that can be applied at the input of an op-amp.

For uA741 this range is $+13V$ to $-13V$ if $\pm V = \pm 15V$ and $T_A = 25^\circ C$.

Output Voltage Range

As seen in the above example of voltage follower, the maximum output voltage swing is limited by the input voltage range.

If opamp is operated as inverting or non-inverting amplifier, output voltage can be more than input voltage (gain). The output voltage swing depends on supply voltages and the output circuit of opamp.

In most of the op-amps output voltage swing is approximately taken 1V less than the supply voltage.

For 741 opamp with $\pm V = \pm 15V$, output voltage swing is typically $\pm 14V$, when $R_L \geq 10k\Omega$.
For $R_L < 10k\Omega$ output voltage swing reduces.

COMMON MODE REJECTION

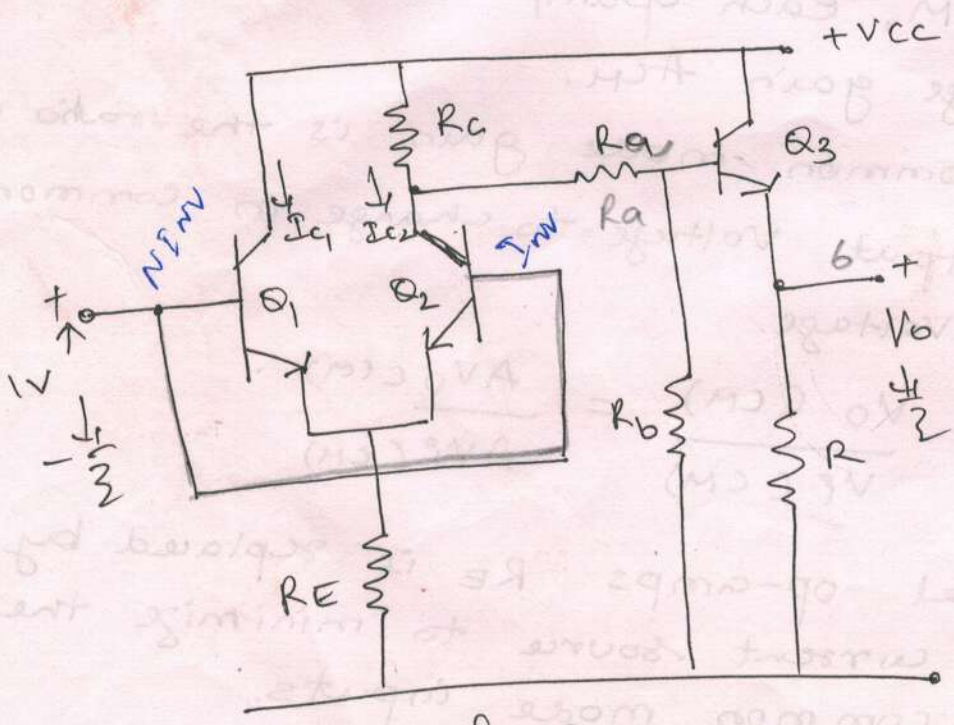


fig (3)

From the above diagram, it can be seen that the two input terminals are shorted together and is raised to 1V above ground level. This voltage is known as common mode Input.

Since there is no differential input, and both inputs being at same potential, ideally output should be zero.

Since Base voltages of Q_1 and Q_2 are raised by 1V above ground, the voltage drop across R_E also increases by +1V. This increases I_{C_1} and I_{C_2}. This increased I_{C_2} produces increased voltage drop across R_C which moves the output voltage to change.

Illy if -1V common mode i/p is applied, I_{C_2} falls and again produces a change in the output voltage.

So in addition to open loop differential input gain M, each opamp has a common mode voltage gain A_{CM}.

The common mode gain is the ratio of change in output voltage to change in common mode input voltage.

$$A_{CM} = \frac{V_{O(CM)}}{V_{i(CM)}} = \frac{AV_{O(CM)}}{AV_{i(CM)}}$$

In practical op-amps R_E is replaced by a constant current source to minimize the effect of common mode inputs.

Even with such circuitry, common mode signal still have some effects on the output.

The success of op-amp to reject the common mode signal is referred to as common mode Rejection Ratio [CMRR]

It is defined as the ratio of differential mode gain (open loop gain M) to the common mode gain A_{CM}.

$$CMRR = \frac{A_d}{A_{CM}} = \frac{M}{A_{CM}} = \infty$$

CMRR is expressed in decibels (dB)

$$CMRR = 20 \log \frac{M}{A_{CM}} \text{ dB}.$$

The effect of common mode gain can be modified with feedback, similar to open loop differential gain is modified to give a closed loop gain.

Consider the NI amplifier shown in fig (4)

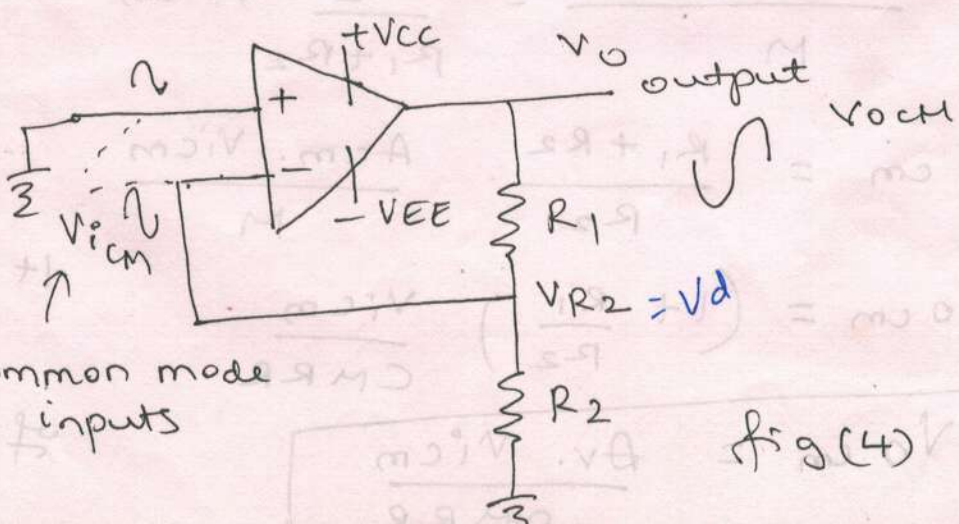


fig (4)

Since the input is grounded, output V_o should be 0. Assume a sine wave signal (noise) is picked up at both inputs as shown in fig (4). This is a common mode input.

The output voltage is

$$V_{O(CM)} = A_{CM} V_{i(CM)}$$

This output voltage will produce a feedback voltage across R_2. This results in a differential voltage at the opamp input terminals. The differential i/p produces an output which tends to cancel the output voltage which causes the feedback.

The differential input voltage required to cancel V_{ocm} is

$$V_d = \frac{V_{O(cm)}}{M} = \frac{A_{cm} \times V_{i\,CM}}{M}$$

V_d is also the feedback voltage developed across R_2,

$$\therefore V_d = \frac{V_{O(CM)} \cdot R_2}{R_1 + R_2} = \frac{R_2}{R_1 + R_2} V_{O(cm)}$$

$$\therefore \frac{A_{cm} \cdot V_{i\,cm}}{M} = \frac{R_2}{R_1 + R_2} V_{O\,cm}$$

$$V_{O\,cm} = \frac{R_1 + R_2}{R_2} \cdot \frac{A_{cm} \cdot V_{icm}}{M}$$

$$V_{O\,cm} = \left(1 + \frac{R_1}{R_2}\right) \frac{V_{icm}}{CMRR}$$

$1 + \frac{R_1}{R_2} = A_V$ ↓ Voltage gain of NI amplifier

$$\therefore V_{O\,cm} = \frac{A_V \cdot V_{icm}}{CMRR}$$

Ex: A 741 opamp used in a NI amplifier with a voltage gain of 50. calculate the output voltage that would result from a common mode input with a peak of 100mV. & CMRR = 90dB.

$$CMRR = 90\ dB$$

$$20 \log_{10} CMRR = 90\ dB$$

$$CMRR = \text{antilog } \frac{90}{20}$$

$$CMRR = 31,623$$

$$\therefore V_{o(cm)} = A_V \cdot \frac{V_{i(cm)}}{CMRR} = \frac{50 \times 100 \times 10^{-3}}{31,623}$$

$$V_{o(cm)} = 158\ \mu V$$

Power Supply Voltage Rejection (PSRR)

Variations in V_{CC} and V_{EE} produces some changes at the output. This effect can be reduced by using a constant current source.

The power supply rejection ratio (PSRR) is a measure of how effective the opamp is dealing with variation in supply voltage.

Power supply rejection ratio is defined as the change in output voltage to the change in supply voltage. PSRR is measure by varying one supply voltage and keeping the other supply voltage constant. It has a unit of $\mu V/V$

741 opamp has a PSRR of 30 $\mu V/V$.

Ex:- A 741 opamp uses a ±15V supply with a 2mV, 120Hz ripply voltage superimposed. Calculate the amplitude of the output voltage produced by the power supply ripple.

$$V_o(\text{ripple}) = V_i(\text{ripple}) \times PSRR$$
$$= 2 \times 10^{-3} \times 30 \times 10^{-6}$$
$$= 60nV$$

OFFSET Voltages and current

Consider the voltage follower circuit shown in fig(2). Here the output and inverting input terminal should follow the voltage at the NI terminal. For the output voltage to be exactly equal to input voltage, transistors Q_1 and Q_2 should be perfectly matched.

The output voltage V_o is

$$V_o = V_{BE_2} = V_i - V_{BE_1}$$
$$\therefore V_o = V_i - V_{BE_1} + V_{BE_2}$$

when $V_i = 0$, only when $V_{BE_1} = V_{BE_2}$, then $V_o = 0$.

In a practical opamp, the two transistors will not be perfectly matched, although in integrated circuits the transistors are very well matched, but not perfectly matched.

If $V_{BE_1} = 0.7V$ and $V_{BE_2} = 0.6V$, then with $V_i = 0$,

$$V_o = 0 - 0.7 + 0.1 = -0.1V.$$

This unwanted o/p voltage is known as o/p offset voltage.

To set V0 to 0, the i/p would have to be raised to +0.1 V. This is termed as Input offset voltage (Vos). The 741 opamp has an input offset voltage of 1mV.

Input offset ~~set~~ voltage (V_{io}) is defined as the voltage that should be applied at the input terminals of an opamp to make the output voltage zero, with $V_i = 0$.

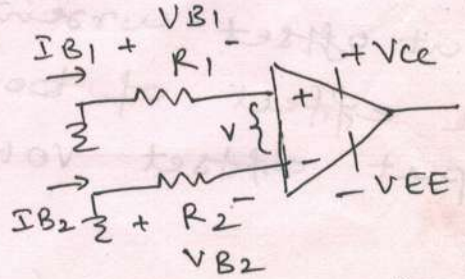
Input offset current

Due to asymmetry in input transistors Q_1 and Q_2 not only there will be change in V_{BE} but also they have different values of h_{fe}. This makes the two base currents to be unequal even with equal collector currents. If one base current is 1 μA and the other is 1.2 μA. The difference between these two currents is known as

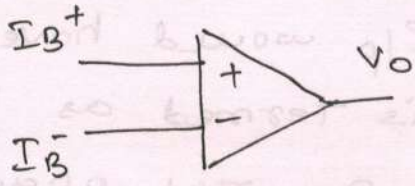
Input offset current (I_{io}) (I_{os})

In the simple voltage follower circuit the input offset current has no effect. If the inputs of opamp are connected with equal values of resistors as shown in fig (5). The unequal base currents of Q_1 and Q_2 produces unequal voltage drops across them which acts like a differential Input signal to produce an output offset voltage.

The typical input offset current for 741 opamp is 20 nA.



$V = I_{B1} R_1 - I_{B2} R_2$.



Due to asymmetry of Q_1 and Q_2, the two base currents are unequal.

let I_B^+ and I_B^- be the two biasing currents (D.C. currents) with input zero, entering N I and Inv terminal of opamp respectively.

The Input bias current is defined as

$$I_{b(av)} = \frac{|I_B^+| + |I_B^-|}{2} \Big/ V_o=0$$

$I_{b(av)}$ is of the order of 100nA.

Since $I_B^+ \neq I_B^-$, the difference of these two biasing currents is called the input offset current,

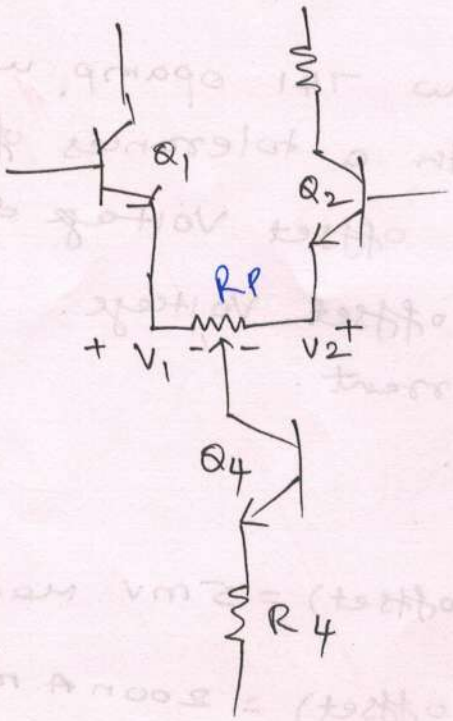
$$I_{io} = |I_B^+| - |I_B^-| \Big/ V_o=0$$

This is of order of 20nA.

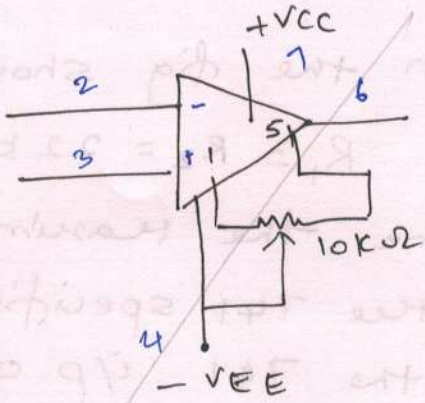
OFFSET Nulling

One method of dealing with input offset voltage and current is shown in fig(6) which shows a low resistance potentiometer R_p connected at the emitter of Q_1 and Q_2. Adjustment of R_p changes the total voltage drop from base to common point at the potentiometer moving contact. Because of an offset voltage is produced by input offset current, this adjustment can null the effect of both input offset current and input offset voltage.

fig(6)



(a) Adjustment of R_P alters the balance of V_1 and V_2



(b) Manufacturers recommended method of offset nulling for 741.

Fig 6(b) shows the manufacturers recommended method of offset nulling for a 741. A low potentiometer is connected to offset nulling terminals 1 and 5 and its moving contact is connected to the -ve supply line. The potentiometer is adjusted to null the output offset voltage to zero, thus nulling both input offset current and input offset voltage.

Resistance Tollerance Effect

It is assumed so far either no resistors at the i/p terminals or equal value of resistors at the i/p terminals. Most op-amp circuits have resistors at the input terminals which may not be of equal values. Even if equal values of resistors are used due to

to their tolerances an o/p offset voltage is produc
This is shown in following example.

Ex:- In the fig shown below 741 opamp uses two resistors $R_1 = R_2 = 22\,k\Omega$. with a tolerances of ±20%. Determine the maximum i/p offset voltage due to
a) the 741 specified i/p offset voltage.
b) the 741 i/p offset current.
c) The resistor tolerance.

(a) For 741 opamp V_i(offset) = 5 mV max.

(b) For 741 opamp I_i (offset) = 200 nA max.

$$V_i(\text{offset}) = I_i(\text{offset}) \times R_1 \text{ or } R_2$$
$$= 200 \times 10^{-9} \times 22 \times 10^3$$
$$= 4.4\ mV$$

c) For 741 opamp, input bias current

I_B = 500nA max.

Resistors have tolerance of ±20%.

$\therefore R_1 = 22k + 20\% = 26.4\,k\Omega$

$R_2 = 22k - 20\% = 17.6\,k\Omega$.

$$\therefore V_i(\text{offset}) = I_B R_1 - I_B R_2 = I_B (R_1 - R_2)$$
$$= 500 \times 10^{-9} (26.4 - 17.6) 10^3$$
$$= 4.4\ mV$$

Input and Output impedances

Input impedance

The input impedance of opamp under open loop is quite high. This input impedance changes with -ve feedback. Most of opamp applications -ve feedback is used.

For NI amplifier, the input impedance with -ve feedback is

$$Z_{if} = Z_i [1 + M\beta]$$

where Z_i = i/p impedance of opamp without f/b
M = open loop opamp gain
β = feedback factor.

Ex:- If $Z_i = 0.3\ M\Omega$, $M(min) = 50,000$, $\beta = 0.1$

$$Z_{if} = Z_i [1 + M\beta] = 0.3 \times 10^6 [1 + 50,000 \times 0.1]$$
$$= 1500\ M\Omega$$

For voltage follower $\beta = 1$, $Z_{if} = 15000\ M\Omega$

The source impedance of the sources connected at the i/p terminals of op-amp should be small compared to i/p impedance of opamp to avoid loss of signal. Most of the opamp application this condition will be true. But there are circuits in which i/p impedance is reduced by the presence of externally connected components.

Output Impedance

741 has typical o/p resistance of 75Ω. If any stray capacitance is in parallel with this, resistor will have a much larger than 75Ω. reactance. So effective o/p resistance is 75Ω.

The o/p impedance of both inverting and non-inverting amplifier with −ve f/b is given by

$$Z_{out} = Z_{of} = \left[\frac{Z_o}{1 + M\beta}\right]$$

where, Z_o = o/p impedance of opamp without feedback.

M = opamp open loop voltage gain

β = feedback factor.

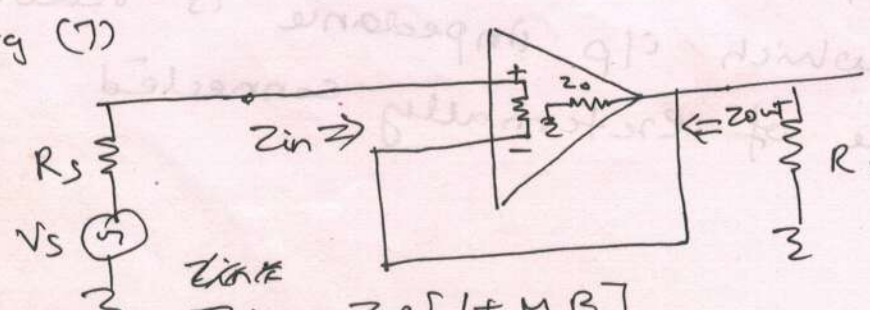
for a voltage follower, $\beta = 1$

For 741 opamp $Z_o = 75\Omega$, $M = 200000$

Then $$Z_{of} = \frac{75}{1 + 200000 \times 1} = 0.0004\,\Omega$$

Load impedance connected at the o/p of an opamp should be much larger than the circuit o/p impedance [fig (7)]. This is to avoid any significant loss of output as a voltage drop across Z_{out}.

fig (7)



$$Z_{out} = \frac{Z_o}{1 + M\beta}$$

$Z_{in} = Z_i [1 + M\beta]$

There is another limit (lower value) that may be connected at the output of an opamp. This depends on the output short circuit curr

Internal current limiting circuitry is included in most of the opamp to protect op-amp from damage that may arise due to short circuit at the output.

For 741 output short circuit current is specified as 25 mA. The maximum o/p current must always be less than this current for satisfactory operation. If a large o/p current is required a power transistor can be used as pass transistor.

Slew Rate and frequency limitations

Slew Rate

The slew rate of an opamp is defined as the maximum rate of change of output voltage with respect to time of a closed loop amplifier when operated under large signal conditions.

A small capacitor (30 pf in 741 opamp) is connected internal to the opamp to avoid opamp breaking into unwanted oscillations at high frequencies. Such opamps are called internal frequency Compensated opamps. This capacitor limits the maximum rate at which the capacitor can be

Consider a voltage follower circuit shown below when input is a sinewave of 10V lower frequency output also will be sinusoidal with a peak of 10V As the frequency of input sine wave increases at a particular frequency output will be distorted and becomes a triangular waveform. The slope of this triangular wave gives the slew rate.

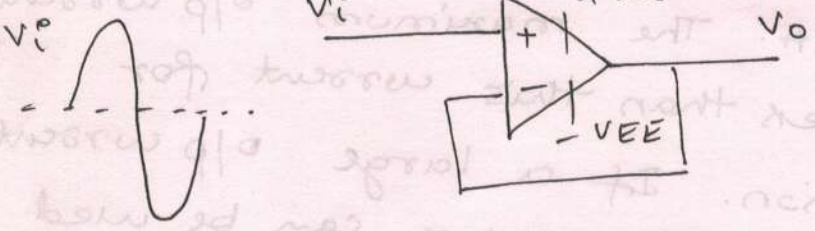
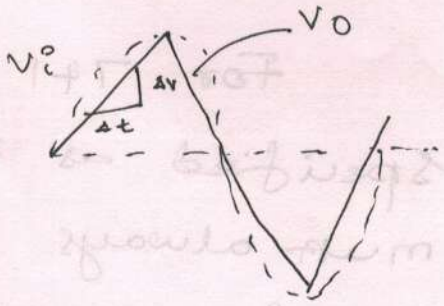


fig (8)



Slew rate

$$S = \frac{\Delta V}{\Delta t} = \frac{dV_o}{dt}.$$

The typical slew rate of 741 is 0.5 V/μs

Ex:- Find the maximum frequency of input sine wave of 10V peak before distortion occurs when applied to a opamp with slew rate of 0.5V/μs

when $V_i = 10 \sin \omega t$

$V_o = 10 \sin \omega t$ voltage follower

$$S = \frac{dV_o}{dt} = 10\omega \cos \omega t$$

$$\frac{0.5V}{10^{-6}s} = 10\,\omega_{max}, \quad \omega_{max} = \frac{0.5}{10 \times 10^{-6}} = 5 \times 10^4 \text{ rad/s}$$

$$2\pi f_{max} = 5 \times 10^4$$

$$f_{max} = \frac{5 \times 10^4}{2\pi}$$

$$f_{max} = 7.958 \text{ KHz}$$

Frequency limitations

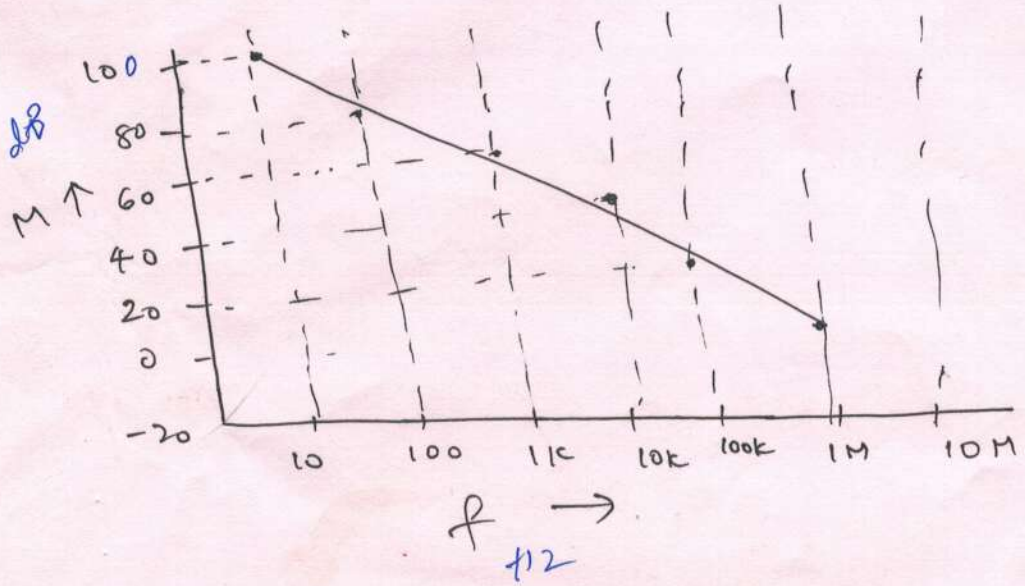
Frequency Response of opamp gives information regarding small signal (low amplitude) behaviour of opamp where a slew rate gives information regarding large signal behaviour of opamp.

Frequency response of opamp is a plot of open loop voltage gain (M) V/s frequency (f).

741 opamp has an open loop voltage gain of 200000, it comes down by 3dB at 5Hz and decreases linearly at a rate of 20dB/decade (decreases by 20dB when frequency change is by 10 times) and crosses the 0dB line at 1MHz known as unity gain cross over frequency.

Since gain bandwidth product of a system is a constant. 741 it is 10^6 Hz [200000 × 5).

Hence opamp is operated with -ve feedback which decreases the gain and increases the B/w.



op-Amp as DC Amplifiers

IC opams makes an excellent direct coupled amplifier. The design of such circuits involves little more than calculation of resistor values for a potential divider. All opamp circuits must provide a current path for the input bias current to each terminal of opamp and all potential dividers should use current levels which are much higher than the input opamp current.

Biasing op-amps

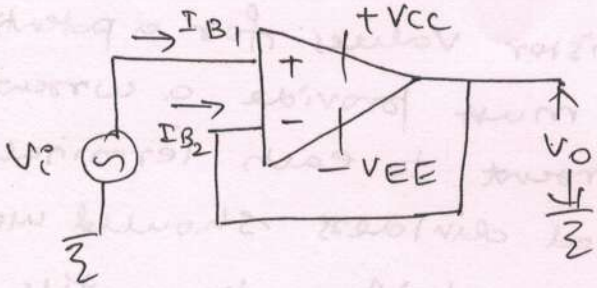
Bias current paths

Like other electronic devices and integrated ckts opamps must be correctly biased if they are to function properly.

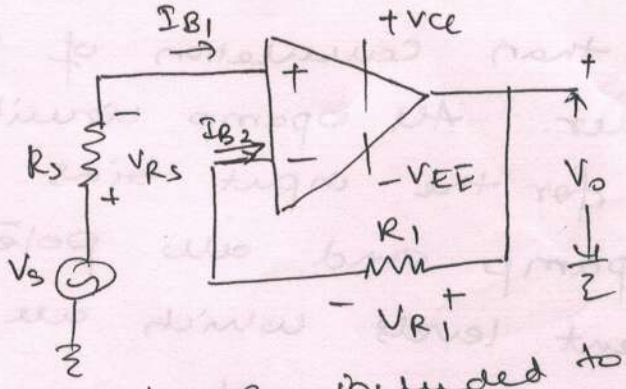
The inputs of most opamps are the base terminals of the transistors in a differential amplifier. Base currents must flow into these terminals for the transistors to be operational. Consequently the i/p terminal must be directly connected to suitable dc bias voltage sources.

For many applications, the most appropriate dc bias voltage level for the opamp input terminals is approximately halfway between the positive and -ve supply voltages. One of the two i/p terminals is usually connected in some way to the output terminals of opamp to facilitate -ve feedback. The other input might be biased directly to ground via signal source as shown in fig 8(a).

Base current I_{B_1} flows into the opamp via the signal source while I_{B_2} flows from the o/p terminals.



(a) Directly connected voltage follower



(b) R_1 included to match R_s

Fig (b) shows a resistor R_1 included in series with the non-inverting to match signal source resistance R_s in series with the non-inverting terminal. The opamp input currents produce voltage drops $I_{B_1} R_s$ and $I_{B_2} R_1$ across the resistors R_s & R_1 should be selected as equal resistors so that the resistor voltage drops are approximately equal. Any difference in these voltage drops will have the same effect as an input offset voltage.

Maximum Bias Resistor Values

If very small values of resistances R_s & R_1 are selected in (fig(b) voltage drops across them will be small on the otherhand if R_s & R_1 are very large, the voltage drops $I_{B_1} R_s$ and $I_{B_2} R_1$ might be several volts. For good bias stabilizing the maximum voltage drops across these resistors must be much smaller than forward V_{BE} drop across opamp input transistors. usually this drop is made $\frac{1}{10}$th of V_{BE}.

i.e. $I_{B(max)} \cdot R_{(max)} = \frac{V_{BE}}{10} = \frac{0.7}{10} = 0.07\,V$

For 741 opamp, $I_{B(max)} = 500\,nA$.

$\therefore R_{(max)} = \frac{0.07}{500 \times 10^{-9}} = 140\,k\Omega$

In general $R_{max} = \frac{0.1\,V_{BE}}{I_{B(max)}}$

Potential Divider bias

The Fig(9) shows a potential divider (R_1 & R_2) employed to derive a terminal bias voltage from the supply voltage. Potential divider bias is normally employed with opams and transistor circuitry. The potential divider current I_2 should be much larger than $I_{B(max)}$ to ensure I_B or any bias current variations has a negligible effect upon the voltage level.

usually $I_2 \geq 100\,I_{B(max)}$, then

$R_1 \simeq \frac{V_{R1}}{I_2}$ & $R_2 \simeq \frac{V_{R2}}{I_2}$

For 741 $I_{B(max)} = 500\,nA$.

$\therefore I_2 = 100 \times 500 \times 10^{-9} = 50\,\mu A$

This is minimum level of I_2. I_2 can be chosen $\simeq 1mA$. Normally in electronic circuits the current are selected as low as possible to minimize the current demand on the power supply.

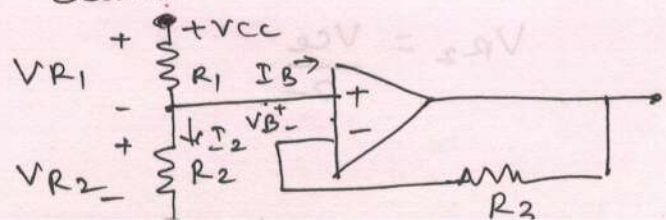


Fig (9)

In fig (9) V_{R_1} and V_{R_2} are usually selected to give V_B closer to ground, or half way between $+V_{CC}$ and $-V_{EE}$. But V_B can be above or below ground level. So long it is with the input voltage range of opamp. For 741 $\pm 12V$ is a supply of ± 15 V.

The resistance R_3 in fig (9) is selected $R_1 \| R_2$ to equalise the voltage drop at the input termina

$$I_{B_1} (R_1 \| R_2) = I_{B_2} R_3$$

$$\therefore R_3 = R_1 \| R_2$$

A single polarity supply voltage can be employe with an opamp. for 741 a +30V supply can be used. As shown in fig (10). In this case the input terminal bias voltage should be approximatel half the supply voltage ($\pm 15V$) but V_B must be within the input voltage range of $\pm 12V$. In fig(the dc o/p voltage will be equal to the bia voltage level being a voltage follower.

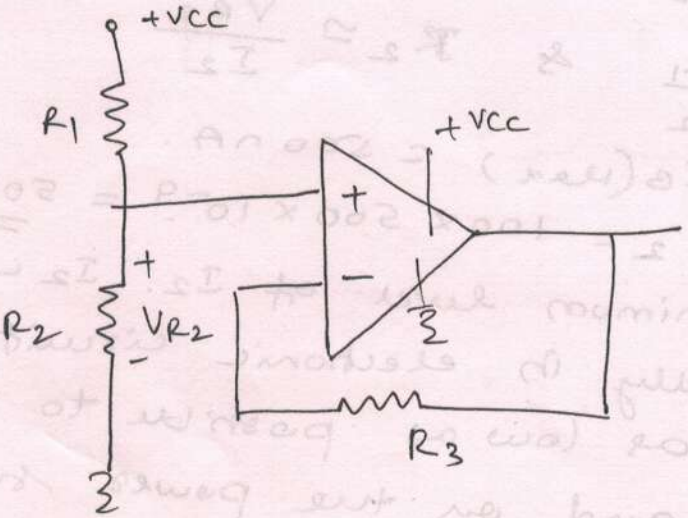


fig (10)

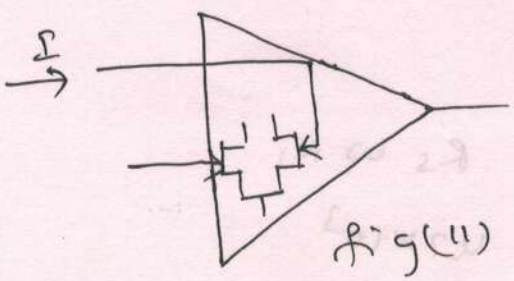
$$V_{R_2} = \frac{V_{cc}}{2}$$

× Biasing BIFET opamps

BIFET opamps are opamps with BIFET input stages as shown in fig (11). They draw very low levels of input bias currents ($\simeq$ 50pA) ie they offer very high input impedance. In this case, the usually design approach of selecting resistor currents (100 × $I_{B(Max)}$) would result in very large value of resistors which are undesirable in several reasons.

1. When the bias resistors at the gate terminal of a FET are extremely large. A charge can accumulate at the gate and this might take a long time to discharge. This makes the gate voltages unstable and the opamp bias conditions would be uncertain.

2. If these values of resistor becomes large. The stray capacitance becomes more effective as resistance values increases which may result in unwanted circuit oscillations.



fig(11)

For satisfactory operations using BIFET opamps the resistance looking out of each input terminals should normally not to exceed 1MΩ.

Direct Coupled Voltage Follower

An opamp can be connected as a voltage follower as shown in fig 8(a). By connecting R_1 in series with the inverting terminal as shown in fig 8(b). It is possible to match with source resistance R_s in series with the non-inverting i/p terminal.

Ex:- A voltage follower using 741 opamp is connected to a signal source via a 47kΩ resistor in fig 8(b). Select a suitable value of resistor R_1. Also calculate the maximum voltage drop across each resistor and the maximum input offset voltage produced by the i/p offset current.

$R_1 = R_s = 47k\Omega$, $V_{Rs} = V_{R_1} = ?$, $V_{i\,offset} = ?$

for 741, $I_{B(max)} = 500nA$, $I_B(typ) = 80nA$

$I_{i(offset)} = 20nA$, $I_{i\,offset(max)} = 200nA$

max voltage drop across each resistor

$V_{Rs} = I_{B(max)} \times R_s$

$= 500nA \times 47k\Omega$

$= 23.5mV$

$V_{R_1} = I_{B(max)} \times R_1$

$= 500nA \times 47k\Omega$

$= 23.5mV$

$V_{i(offset)} = I_{i(offset)} \times R_s$ or R_1

$= 20 \times 10^{-9} \times 47 \times 10^3$

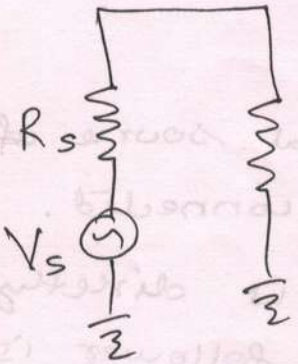
$= 0.94mV$

The i/p and o/p impedances of the voltage follower are

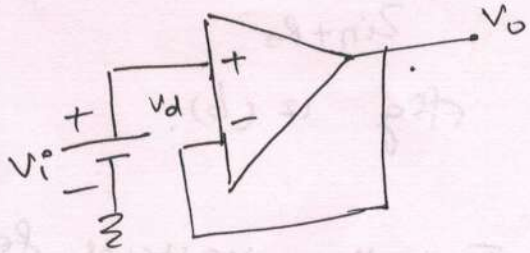
$$Z_{in} = (1+M)Z_i \quad \text{and} \quad Z_{out} = \frac{Z_o}{1+M} \quad [\beta = 1]$$

ie voltage follower has a very high i/p impedance and a very low o/p impedance. It can be used for converting a high impedance source to a low output impedance. ie it can be used as a Buffer between high impedance source and low impedance load. Thus it is termed as buffer amplifier

Fig 12(a) shows the source with impedance R_s being connected directly to the load R_L. Here a signal voltage is potentially divided across R_s & R_L



12(a)



$$V_o = V_d \cdot M$$

$$V_d = \frac{V_o}{M}, \text{ But } V_o = V_f$$

$$V_d = \frac{V_i}{M} \quad \text{since } M \gg 1 \quad V_o \simeq V_i$$

$$V_i - V_d - V_o = 0$$

$$V_o = V_i - V_d$$

$$V_o = V_i - \frac{V_i}{M}$$

$$\boxed{V_o = V_i\left[1 - \frac{1}{M}\right]}$$

Fig 12(b) shows the voltage follower which presents a very high i/p impedance to the signal source.

I/p voltage V_i is

$$V_i = \frac{Z_{in}}{Z_{in}+R_s} \times V_s$$

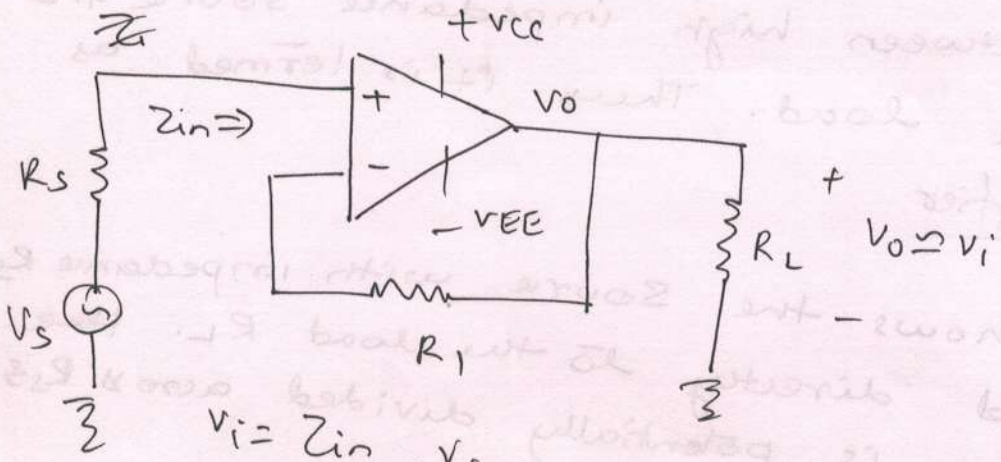
$Z_{in} >> R_S \quad \therefore V_i \simeq V_S$

The o/p voltage V_o is

$$V_o = V_i \left[1 - \frac{1}{M}\right]$$

$$V_L = \frac{R_L}{R_L + Z_{out}} V_o$$

Since $R_L >> Z_{out}$, $V_L \simeq V_o$



$$V_i = \frac{Z_{in}}{Z_{in} + R_S} \cdot V_S$$

fig 12 (b).

Ex:- For the voltage follower a signal source of 1V and $R_S = 47k\Omega$ and $R_L = 20k\Omega$ is connected. Calculate the voltage (a) when load is directly connected to source (b) when the voltage follower is between the load and source.

$R_S = 47k\Omega$, $R_L = 20k\Omega$, $M = 200,000$

$Z_i = 2M\Omega$, $Z_o = 75\Omega$

(a) $$V_L = \frac{V_S \cdot R_L}{R_L + R_S} = \frac{1 \times 20 \times 10^3}{20 \times 10^3 + 47 \times 10^3} = 298\,mV$$

(b) $Z_{in} = (1+M)\, Z_i$

$= (1+200{,}000)\ 2\ M\Omega$

$= 4 \times 10^{11}\ \Omega$

$$V_i = \frac{V_s \cdot Z_{in}}{R_s + Z_{in}} = 0.999 \simeq 1V$$

$$V_o = \left(1 - \frac{1}{M}\right) V_i = 1\left(1 - \frac{1}{200000}\right) = 1V$$

$$Z_{out} = \frac{Z_o}{1+M} = \frac{75}{1+200{,}000} = 37 \times 10^{-5}\ \Omega$$

$$V_L = V_o \cdot \frac{R_L}{R_L + Z_{out}} = \frac{1 \times 20 \times 10^3}{20 \times 10^3 + 37 \times 10^{-5}}$$

$= 1V$

Voltage follower with a potential divider

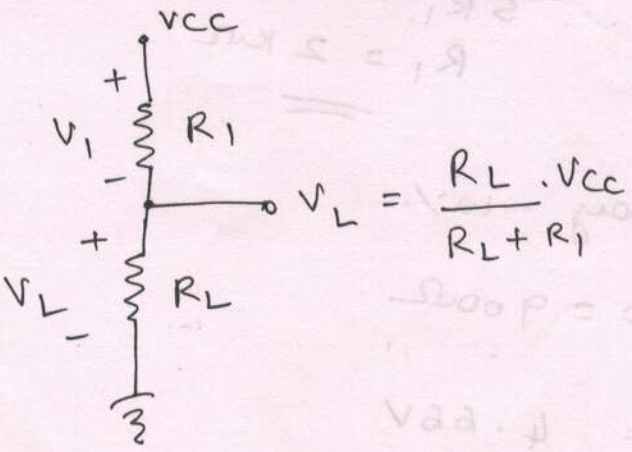


fig 13(a)

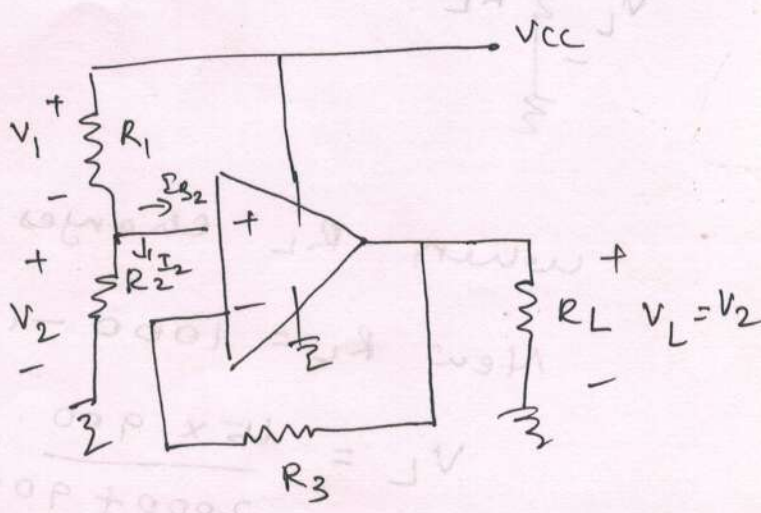


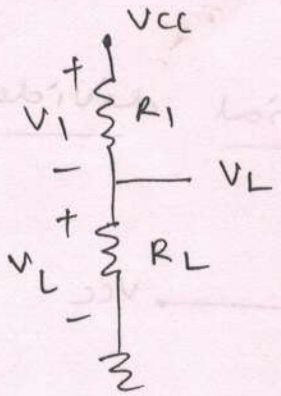
fig 13(b)

The above fig shows use of a voltage follower with a potential divider to produce a low impedance dc voltage source.

In Fig 13(a) R_L is connected directly in series with R_1 to derive a voltage V_L from the supply V_{cc}, in this V_L varies with R_L.

In fig 13(b), the presence of voltage follower maintains the load voltage constant regardless of R_1

prob A 1kΩ load is to have 5V developed across it from 15V source. Design a suitable circuit as shown in fig 13(a) & (3(b). Calculate the load voltage variation in each case when R_L varies by −10%. use 741 opamp.



$$V_L = \frac{R_L}{R_1 + R_L} \cdot V_{cc} = \frac{1000}{R_1 + 1000} \times 15 = 5$$

$$\therefore 5R_1 + 5000 = 15000$$

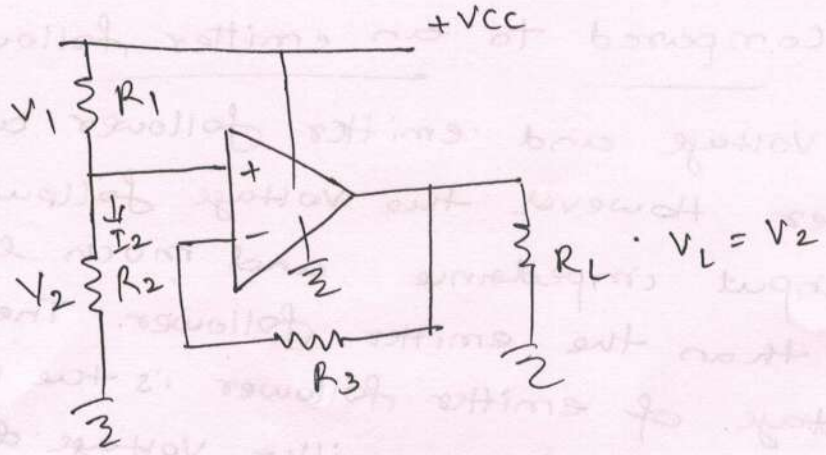
$$\therefore 5R_1 = 10000$$

$$R_1 = 2\,k\Omega$$

when R_L changes by −10%.

New $R_L = 1000 - 100 = 900\Omega$

$$V_L = \frac{15 \times 900}{2000 + 900} = 4.66V$$



from fig $V_2 = V_L = 5\,V$

$$V_1 = V_{cc} - V_L = 15 - 5 = 10V$$

For 741, $I_{B(Max)} = 500\,nA$

let $I_2 = 100\, I_{B(Max)} = 100 \times 500 \times 10^{-9}$

$$I_2 = 50\,\mu A$$

$$V_2 = V_L = 5 = R_2 I_2$$

$$\therefore R_2 = \frac{5}{I_2} = \frac{5}{50 \times 10^{-6}} = 100\,k\Omega$$

$$R_1 = \frac{V_1}{I_2} = \frac{10}{50 \times 10^{-6}} = 200\,k\Omega$$

when R_L changes by -10%.

$$R_L = 900\Omega$$

$V_L = V_2 = 5V$ $\therefore$ it is independent of R_L.

Voltage follower compared to an emitter follower

Both voltage and emitter follower are used as Buffer amplifier. However the voltage follower has a much higher input impedance and much lower output impedance than the emitter follower. The most obvious disadvantage of emitter follower is the dc voltage loss due to the transistor base-emitter voltage drop as shown in fig 14(a). The dc voltage follower has dc loss of $\frac{V_i}{M}$ which is insignificant. in fig 14(b). The a.c signal loss is more in emitter follower because lower input impedance and higher o/p impedance compared to voltage follower.

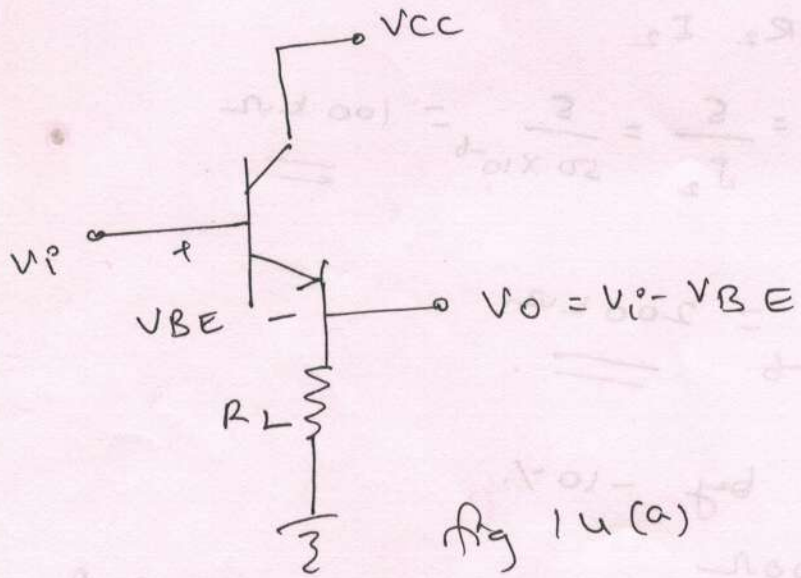
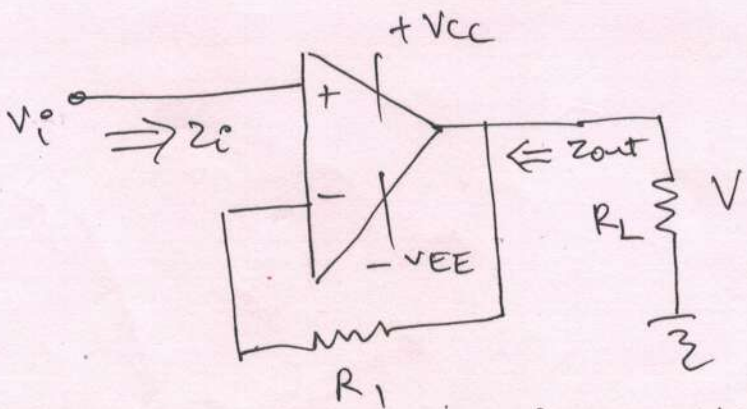


fig 14(a)



$V_o = V_i\left[1 - \frac{1}{A}\right]$

fig 14(b)

Direct coupled Non-Inverting amplifier

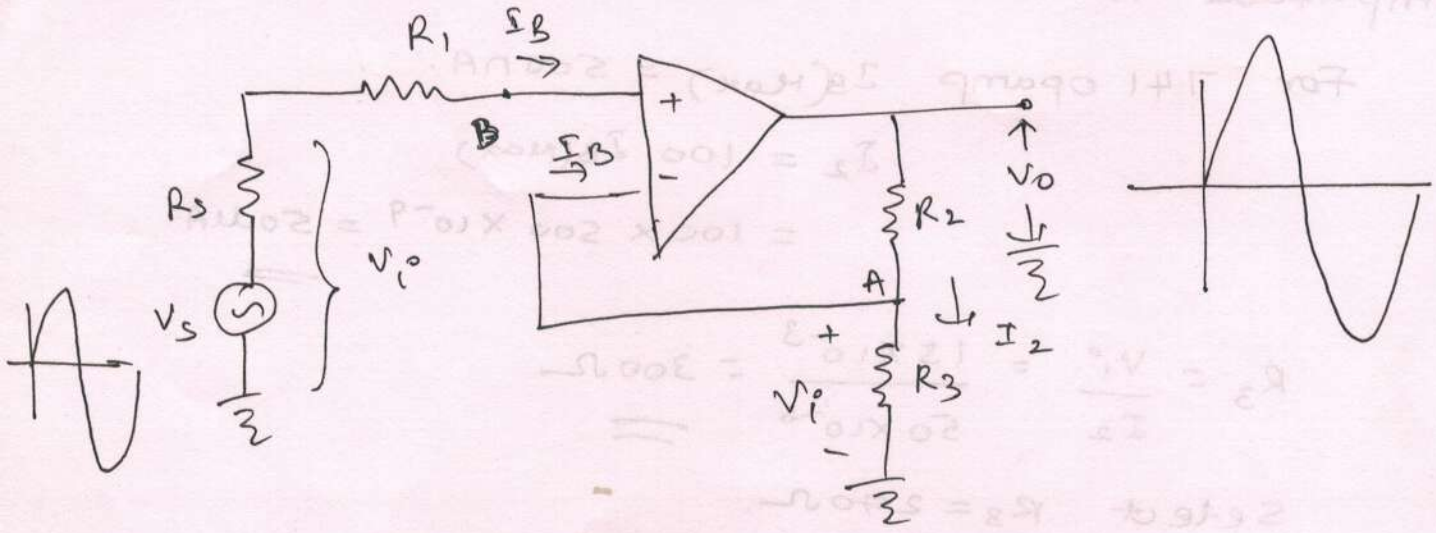


fig (15)

Here, $V_i = I_2 \cdot R_3$, $V_o = I_2 (R_2 + R_3)$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{I_2 (R_2 + R_3)}{I_2 R_3} = 1 + R_2/R_3$$

$$\& \quad R_3 = \frac{V_i}{I_2}$$

with Bipolar input opamp. $I_2 >> I_{B\,max}$

with BIFET opamp largest value of resistor is chosen as 1MΩ.

In each case, potential divider resistor values are then determined using V_i, V_o and I_2.

To equalise the $I_B R$ voltage drops at the opamp inputs, $R_1 = R_2 \,||\, R_3$ if $R_1 >> R_s$

otherwise $(R_s + R_1) = R_2 \,||\, R_3$

Ex: Using 741 opamp design a Non-inverting amplifier to have a voltage gain of ≅66. The signal amplitude is 15 mV.

For 741 opamp $I_{B(Max)} = 500\,nA$.

$$I_2 = 100\, I_{B(Max)}$$

$$= 100 \times 500 \times 10^{-9} = 50\,\mu A$$

$$R_3 = \frac{V_i^\circ}{I_2} = \frac{15 \times 10^{-3}}{50 \times 10^{-6}} = 300\,\Omega$$

Select $R_3 = 270\,\Omega$.

$$I_2 = \frac{V_i^\circ}{R_3} = \frac{15 \times 10^{-3}}{270} = 55.6\,\mu A$$

$$V_o = A_V \cdot V_i^\circ = 66 \times 15 \times 10^{-3} = 990\,mV$$

&

$$V_o = I_2 (R_2 + R_3)$$

$$R_2 + R_3 = \frac{V_o}{I_2} = \frac{900 \times 10^{-3}}{55.6 \times 10^{-6}} = 17.8\,k\Omega$$

$$R_2 + R_3 = 17.8\,k\Omega$$

$$R_2 = 17.8 \times 10^3 - 270$$

$$R_2 = 17.53\,k\Omega$$

Use $R_2 = 18\,k\Omega$

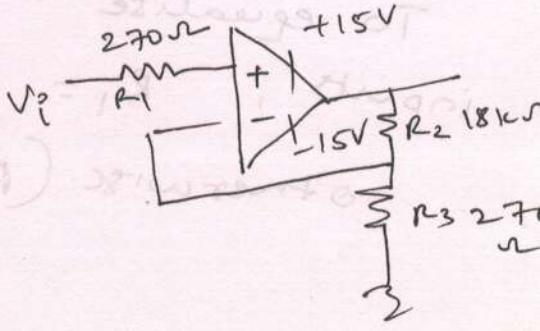
$$V_o = (R_2 + R_3)\, I_2 = (18000 + 270)\, 55.6 \times 10^{-6}$$

$$= 1015.81\,mV = 1.01\,V$$

$$R_1 = R_2 \,||\, R_3$$

$$R_1 = 18000 \,||\, 270$$

$$R_1 \cong 270\,\Omega$$



Ex: Redesign the non-inverting amplifier using BIFET opamp LF 353.

For LF353, $I_{B(max)} = 200\,pA$.

If $R_3 = \frac{V_i}{I_2}$ $\quad I_2 = 100\, I_{B(max)}$

$= 100 \times 200 \times 10^{-12}$

$= 2 \times 10^{-8} A$.

$\therefore R_3 = \frac{15 \times 10^{-3}}{2 \times 10^{-8}} = 7.5 \times 10^5 \Omega$

Then $V_o = (R_2 + R_3) I_2$

$(R_2 + R_3) = \frac{V_o}{I_2} = \frac{A_v \cdot V_i^o}{I_2} = \frac{66 \times 15 \times 10^{-3}}{2 \times 10^{-8}}$

$R_2 + R_3 = 495 \times 10^5$

$R_2 + R_3 = 49.5\,M\Omega$

$R_2 = [49.5 - 0.75]\,M\Omega$

$= 48.75\,M\Omega$ which is very large.

$\therefore$ choose $R_2 = 1M\Omega$

wkt $A_v = 1 + \frac{R_2}{R_3} = 66$

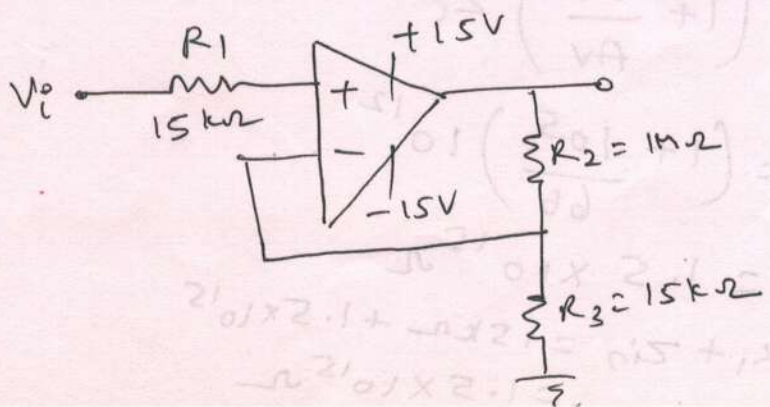
$\frac{R_2}{R_3} = 65$ $\quad \therefore R_3 = \frac{65}{R_2}$ $\quad R_3 = \frac{R_2}{65} = \frac{1M}{65}$

$R_3 = 15.38\,K\Omega$

Choose $\boxed{R_3 = 15\,K\Omega}$

$R_1 = R_2 \,||\, R_3 = 1M\Omega \,||\, 15K\Omega$

$R_1 = 15K\Omega$



The input impedance

$$Z_{in} = (1 + m\beta) Z_i$$

$$\beta = \frac{R_3}{R_2 + R_3} = \frac{1}{A_V}$$

∴ for NI amp

$$\boxed{Z_{in} = \left[1 + \frac{M}{A_V}\right] Z_i}$$

As shown in fig(16) if R_1 is also included, the input impedance Z_{in}' as seen by the source is

$$Z_{in}' = Z_{in} + R_1$$

Normally,

$Z_{in} >> R_1$,

$\therefore Z_{in}' \simeq Z_{in}$

$$Z_{out} = \frac{Z_o}{1 + M\beta},$$

$$Z_{out} = \frac{Z_o}{1 + \frac{M}{A_V}}$$

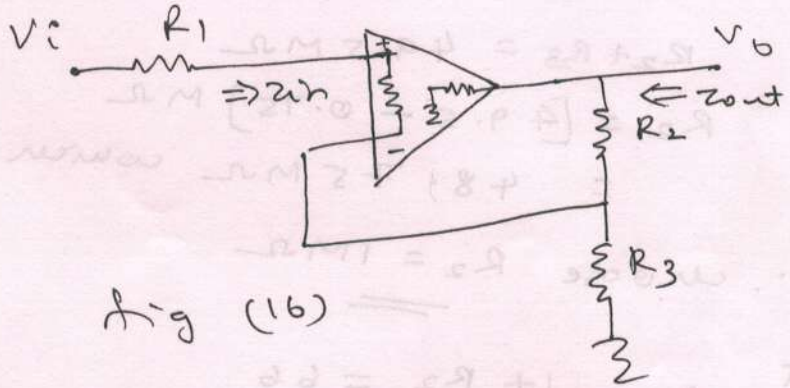


fig (16)

Ex:- Calculate input and output impedance of NI amplifier using LF 353 opamp.

for LF 353, $M = 100000$, $Z_i = 10^{12}\,\Omega$

$$Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i$$

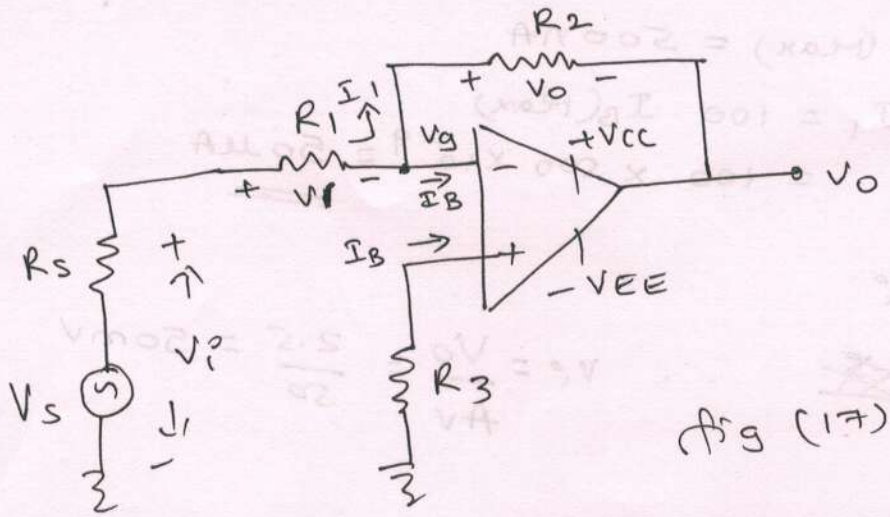
$$Z_{in} = \left(1 + \frac{10^5}{66}\right) 10^{12}$$

$$Z_{in} = 1.5 \times 10^{15}\,\Omega$$

$$Z_{in}' = R_1 + Z_{in} = 15k\Omega + 1.5 \times 10^{15}$$

$$= 1.5 \times 10^{15}\,\Omega$$

Direct Coupled inverting Amplifier



V_g = virtual ground

Fig (17)

Fig (17) shows a Direct coupled inverting amplifier. Resistor R_3 is included to equalize the dc voltage drop due to the input bias currents. TO equalise these drops equal resistors should be seen looking out from each i/p terminals of the opamp.

$\therefore R_3 = R_1 \parallel R_2$

If Rs is comparable to R_1, then

$R_3 = (R_1 + R_S) \parallel R_2$

with bipolar opamp I_1 is first selected such that

$I_1 >> I_{B(max)}$

with BIFET opamp, the largest value resistor is first selected as 1MΩ then

$$R_1 = \frac{V_1}{I_1} \quad \& \quad R_2 = \frac{V_o}{I_1}$$

Ex:- Design an inverting amplifier using 741 opamp. The voltage gain is to be 50 and the output voltage amplitude is to be 2.5V.

For 741, $I_{B(max)} = 500nA$

$$I_1 = 100\ I_{B(max)}$$
$$= 100 \times 500 \times 10^{-9} = 50\mu A$$

$$V_o = A_v \cdot V_i$$

$$A_v = \frac{V_o}{V_i} = \frac{2.5}{V_i} \quad \therefore \quad V_i = \frac{V_o}{A_v} = \frac{2.5}{50} = 50mV$$

Let $V_i = V_1$

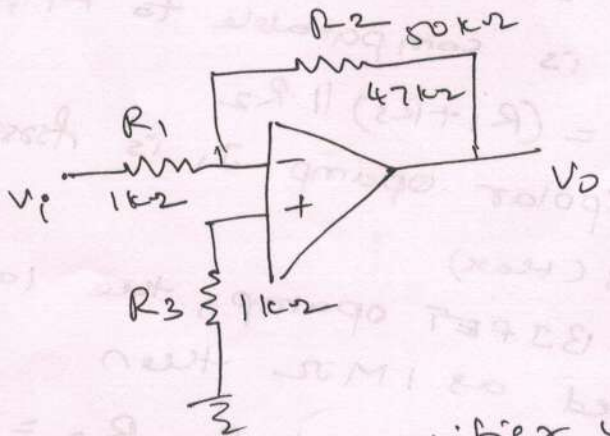
$$\therefore R_1 = \frac{V_1}{I_1} = \frac{50 \times 10^{-3}}{50 \times 10^{-6}} = 1k\Omega$$

$$R_2 = \frac{V_o}{I_1} = \frac{2.5}{50 \times 10^{-6}} = 50k\Omega$$

use $R_2 = 47k\Omega$ or $47k\Omega + 3.3k\Omega$

$$R_3 = R_1 \parallel R_2 = 1k\Omega \parallel 50k\Omega$$

$$R_3 \cong 1k\Omega$$



Ex:- Redesign the inverting amplifier using LF353 BIFET opamp

Select the largest resistors as $1M\Omega$

let $R_2 = 1M\Omega$, $R_1 = \frac{R_2}{A_v} = \frac{1 \times 10^6}{50} = 20k\Omega$

use $R_1 = 18k\Omega$ or $18k\Omega + 2.2k\Omega$

$$R_3 = R_1 \parallel R_2 = 20k\Omega \parallel 1M\Omega \cong 20k\Omega$$

Performance

$Z_{in} = [1 + M\beta] Z_i$ is applicable only to the Non-Inverting amplifier.

For inverting amplifier, because inverting terminal is at virtual ground

$Z_{in} \simeq R_1$

But $Z_{out} = \frac{Z_o}{1 + M\beta}$ where $\beta = \frac{R_1}{R_1 + R_2}$

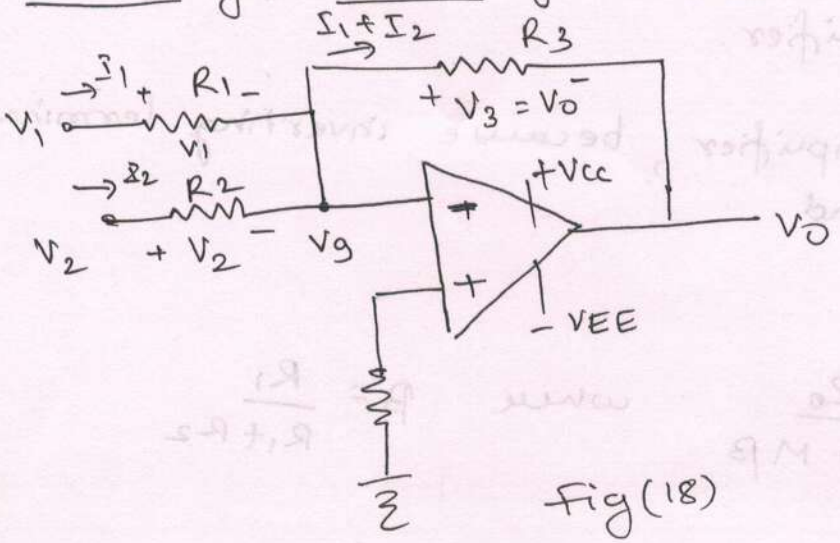
$\therefore Z_{out} = \frac{Z_o}{1 + M \cdot \frac{R_1}{R_1 + R_2}}$

when $R_2 >> R_1$, $Z_{out} = \frac{Z_o}{1 + M\frac{R_1}{R_2}} = \frac{Z_o}{1 + \frac{M}{A_V}}$

as in the case of Non-Inverting amplifier.

Summing Amplifier

* Inverting Summing Amplifier



Fig(18)

Fig(18) shows a summing amplifier with two inputs. This is essentially an inverting amplifier with two input terminals and two input resistors. The inverting terminal being at virtual ground.

$$I_1 = \frac{V_1}{R_1}, \quad I_2 = \frac{V_2}{R_2}$$

Input impedance of opamp being very high, $(I_1 + I_2)$ flows through R_3.

$$\therefore V_o = -(I_1 + I_2) R_3$$

$$V_o = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] R_3$$

$$V_o = -\left[\frac{R_3}{R_1} V_1 + \frac{R_3}{R_2} V_2\right]$$

If $R_1 = R_2$

$$V_o = -\frac{R_3}{R_1}\left[V_1 + V_2\right]$$

But $\frac{R_3}{R_1} = A_V$

$$\therefore V_o = -A_V\left[V_1 + V_2\right]$$

If $R_1 = R_2 = R_3$ then $V_o = -\left[V_1 + V_2\right]$

This shows that output voltage is sum of input voltages with inversion.

If R_3 is greater than R_1 and R_2, then Sum is multiplied by $\frac{R_3}{R_1}$.

If R_3 is less than R_1, then Sum is divided by $\frac{R_1}{R_3}$

Averaging circuit

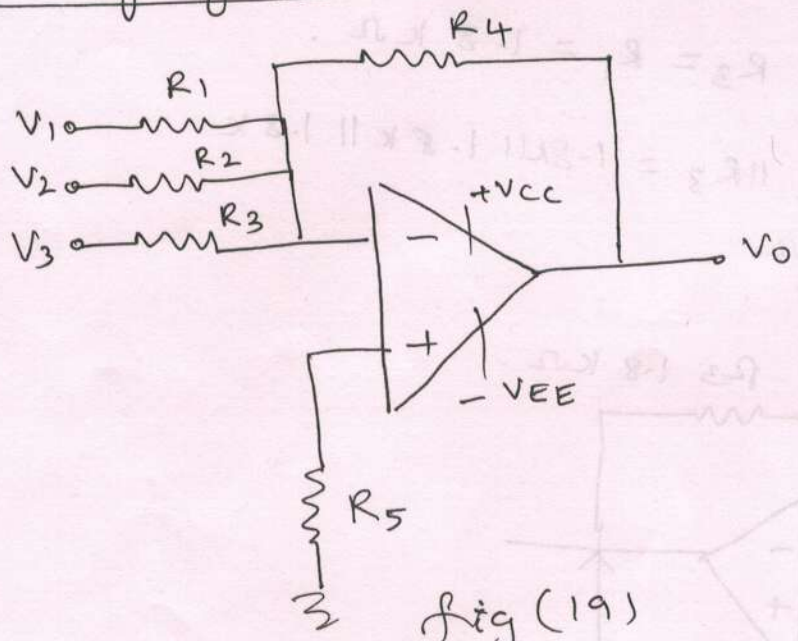


fig (19)

If the summing amplifier has 3 inputs and if $R_1 = R_2 = R_3$ and $R_4 = \frac{R_1}{3}$

then $V_o = -\frac{1}{3}\left[V_1 + V_2 + V_3\right]$

which is the average of the inputs. Thus, Summing amplifier can be used as an averaging circuit.

Ex: Design a summing amplifier to give the direct sum of two inputs which each range from 0.1V to 1V use 741 opamp.

let $I_1(\text{Min}) = 100\, I_B(\text{Max}) = 100 \times 500\ nA = 50\ \mu A$

$$R_1 = \frac{V_1(\text{Min})}{I_1(\text{Min})} = \frac{0.1}{50 \times 10^{-6}} = 2\ K\Omega$$

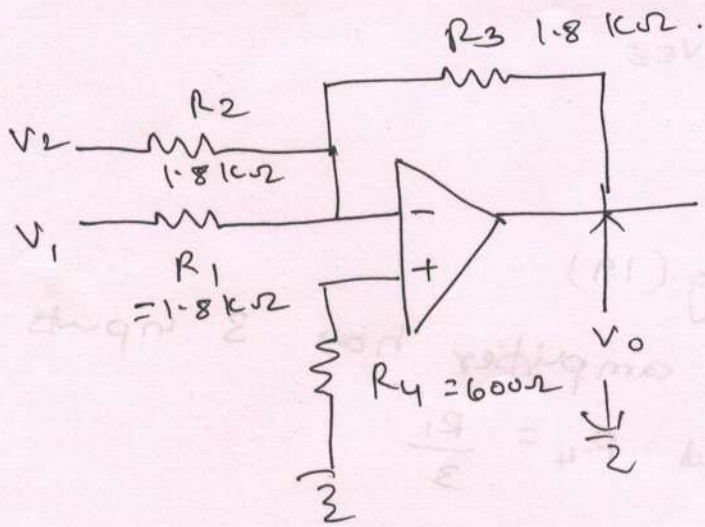
Use $R_1 = 1.8\ K\Omega$.

& $R_1 = R_2 = 1.8\ K\Omega$.

for $A_V = 1$, $R_3 = R_1 = 1.8\ K\Omega$.

$R_4 = R_1 \# R_2 \# R_3 = 1.8K \# 1.8K \# 1.8K$

$= 600\Omega$



The Summing amplifier can be used as a multichannel audio mixer for several audio channels.

Non-Inverting Summing circuit

A Non-inverting amplifier can be employed as a summing circuit as shown in fig(20).

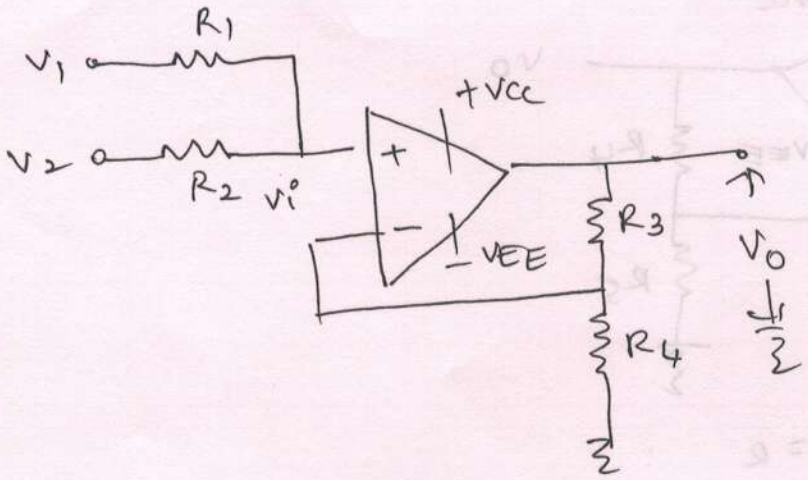
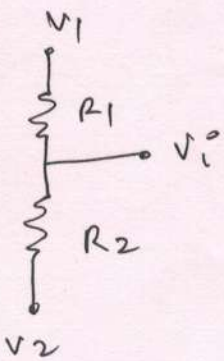


fig (20)

This gives the direct sum of inputs instead of inverted sum. The expression or output voltage can be obtained by applying superposition theorm at NI terminal.



$$V_i^\circ = \frac{R_2}{R_1+R_2} V_1 + \frac{R_1}{R_1+R_2} V_2$$

If $R_1 = R_2 = R$

$$V_i^\circ = \frac{V_1 + V_2}{2}$$

olp of non-inverting amplifier is

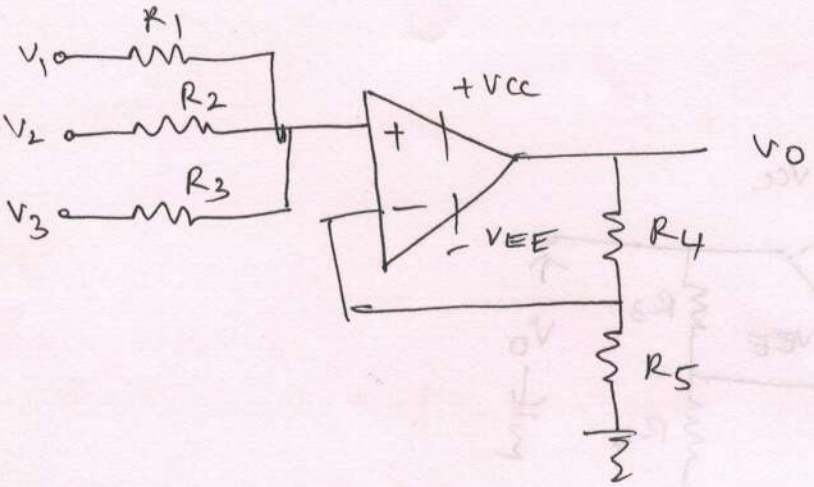
$$V_0 = \left(1 + \frac{R_3}{R_4}\right) V_i^\circ = \left(1 + \frac{R_3}{R_4}\right)\left(\frac{V_1+V_2}{2}\right)$$

If $R_3 = R_4 = R$

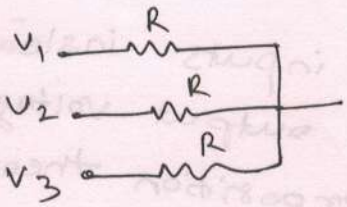
$$V_0 = (1+1)\left(\frac{V_1+V_2}{2}\right)$$

$$\boxed{V_0 = V_1 + V_2}$$

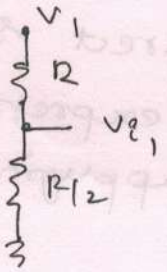
Three input NI Summing circuit is shown in fig (21)



If $R_1 = R_2 = R_3 = R$



when $V_2 = V_3 = 0$



$$V_{i_1} = \frac{R/2}{R + R/2} \cdot V_1$$

$$V_{i_1} = \frac{V_1}{3}$$

III^ly when $V_1 = V_3 = 0$, $V_{i_2} = V_2/3$,

when $V_1 = V_2 = 0$, $V_{i_3} = V_3/3$

By Superposition theorm

$$V_i = V_{i_1} + V_{i_2} + V_{i_3} = \frac{V_1 + V_2 + V_3}{3}$$

o/p of NI amplifier

$$V_0 = \left(1 + \frac{R_4}{R_5}\right) V_i = \left(1 + \frac{R_4}{R_5}\right)\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

If $R_4 = 2R_5$

Then $V_0 = \frac{3}{3}(V_1 + V_2 + V_3)$

$$\boxed{V_0 = V_1 + V_2 + V_3}$$

Difference Amplifier

A difference amplifier or a differential amplifier, amplifies the difference between the two input signals. An IC opamp is basically a difference amplifier having inverting and NI input. But the open loop voltage gain is too large to be used without feedback. Hence practical difference amplifier should have -ve feedback.

The circuit of difference amplifier circuit is shown in fig (21).

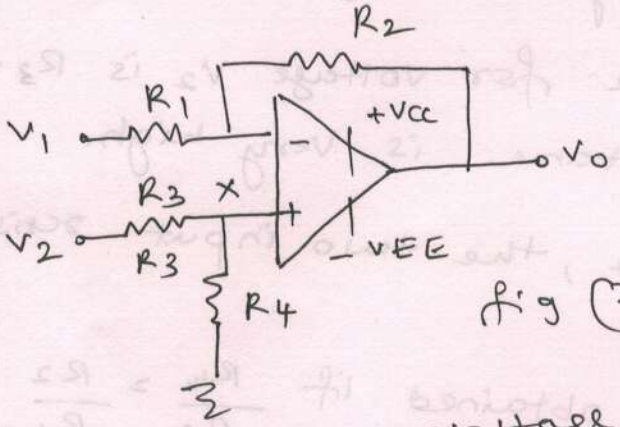
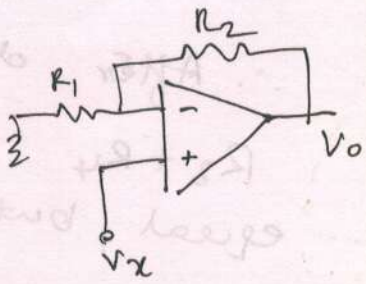


fig (21)

To find o/p voltage V_o

Case (i) when $V_2 = 0$, $V_x = 0$, $V_{o1} = -\frac{R_2}{R_1} V_1$

Case (ii) when $V_1 = 0$ $V_x = \frac{R_4}{R_3 + R_4} \cdot V_2$



$$V_{o2} = \left(1 + \frac{R_2}{R_1}\right) V_x$$

$$= \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_2$$

let $R_1 = R_3$; $R_2 = R_4$ or $R_4/R_3 = R_2/R_1$

$$V_{o2} = \frac{R_3 /\!\!/ R_4}{R_3} \cdot \frac{R_4}{R_3 /\!\!/ R_4} V_2 = \frac{R_4}{R_3} V_2 = \frac{R_2}{R_1} V_2$$

$\therefore V_o = V_{o1} + V_{o2}$

$$V_o = \frac{-R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2$$

$$\boxed{V_o = \frac{R_2}{R_1}\left[V_2 - V_1\right]} \quad \text{—— (1)}$$

If $R_1 = R_2$, $V_o = V_2 - V_1$ acts as a subtractor.

Input Resistances

The input resistance for voltage V_1 in fig (21) is R_1 as in the case of inverting amplifier.

The i/p resistance for voltage V_2 is $R_3 + R_4$ as opamp input resistance is very high.

If $R_1 = R_3$ and $R_2 = R_4$, the two input resistances are unequal.

$\therefore$ Equation (1) can be obtained if $\frac{R_4}{R_3} = \frac{R_2}{R_1}$ instead of $R_1 = R_3$ and $R_2 = R_4$.

$\therefore$ After determining R_1, R_1 can be made equal to $R_3 + R_4$ which makes both input resistances equal, but $\frac{R_4}{R_3} = \frac{R_2}{R_1}$

Even if $R_1 = R_3$ and $R_2 = R_4$ and the two input resistances R_1 and $(R_3 + R_4)$ are not equal, this difference doesnot matter if the source resistances are small compared to input resistances.

If $R_3 = R_1$ & $R_4 = R_2$ the resistance looking out of each input will be equal. ie $(R_3 \| R_4) = (R_1 \| R_2)$

This minimizes the input offset voltage.

The differential mode i/p resistance $R_{i\,diff}$ is the resistance offered to the signal source which is connected directly across the input terminals. It is the sum of two resistances.

$$R_{i\,(diff)} = R_1 + R_3 + R_4.$$

The common mode i/p resistance is the resistance offered to a signal source which is connected between ground and both input terminals ie the parallel combination of the two input terminals.

$$R_{i\,(cm)} = R_1 \,||\, (R_3 + R_4)$$

Common mode voltages

Eq(1) shows that the o/p voltage is the amplified difference of the two input voltages. If a common mode input voltage V_n is present then two input voltages will be $V_1 + V_n$ and $V_2 + V_n$ and at the output V_n will be cancelled out, when the difference of the two inputs is amplified

For Eq(1) $\frac{R_4}{R_3} = \frac{R_2}{R_1}$, If these two ratios are not exactly same, one input voltage is amplified by a greater amount than the other. Also the Common mode voltage V_n also gets amplified by greater amount than at the other input. with the Common mode voltages will not be completely cancelled which produces a common mode o/p voltage.

One way of minimizing the common mode o/p is to use a small variable resistor in series with R_4 so that $\frac{R_4}{R_3}$ can be made approximately equal to $\frac{R_2}{R_1}$ and common mode o/p can be made zero. as shown in fig (22).

Output level shifting

In fig (22) if R_4 is connected to a bias voltage V_B instead of being grounded, if both input voltages are zero, the voltage at the NI terminal is

$$V_+ = \frac{R_3}{R_3 + R_4} V_B$$

Since i/p impedance of opamp is very high

$$V_- = V_+$$

and output is, $V_o = \left(1 + \frac{R_2}{R_1}\right) V_+$

$$V_o = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{V_B}{1 + R_4/R_3}\right)$$

If $\frac{R_4}{R_3} = \frac{R_2}{R_1}$ $\boxed{V_o = V_B}$

If V_B is adjustable then o/p dc voltage level can be shifted as desired.

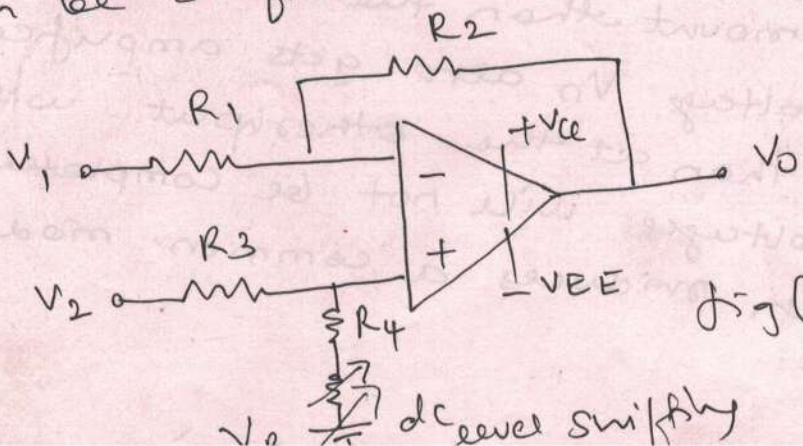


fig (22)