Op Amp as Non-Linear Circuit

Operational amplifiers are widely used in circuits in which the output is switched between the +ve and -ve saturation levels. Positive feed back is employed in these circuits.

Generally, $+V_{sat} \simeq (V_{cc} - 1V)$

$-V_{sat} \simeq (-V_{EE} + 1V)$

The 1V difference may change from op-amp to op-amp. For very small change in input voltage, the op-amp output switches from $+V_{sat}$ to $-V_{sat}$.

Input Voltage Range:

In linear applications, -ve feedback keeps the op amp input terminal voltages closely equal. In switching applications, the dc voltage level at one input terminal is different from that at the other input terminal. The switching application normally employ +ve feedback to provide a substaintial voltage difference between the two input terminals. This ensures that o/p is saturated at either a +ve or -ve voltage level. So, in switching applications, there is normally a differential voltage at the op-amp input terminal.

∴ The minimum differential voltage required to produce output saturation is given by :-

$V_{i(diff)} \simeq \dfrac{V_{cc}}{M_{min}}$, where M_{min} = minimum open loop voltage gain of op amp.

For 741 op-amp, $M_{min} \simeq 50,000$

If a $\pm 15V$ supply is used, $V_{i(diff)} = \dfrac{\pm 15V}{50,000} = \pm 300 \, uV$

Most op-amp can accept a differential input voltage equal to twice the supply voltage. The op-amp input stage may be damaged if this maximum is exceeded. For eg: with a $\pm 15V$ supply, the maximum differential input should not exceed 30V.

Op-amp as Comparator

A comparator is a circuit which compares a signal voltage applied at one i/p of an op-amp with a known reference voltage at the other end. and produces either a high or a low output voltage, depending on which i/p is higher.
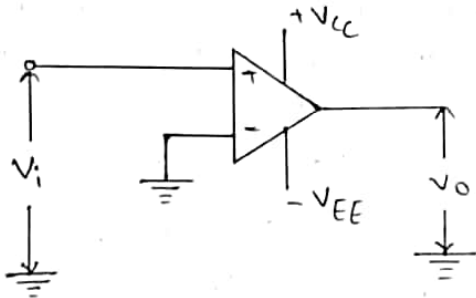
Zero Crossing Detector (ZCD)

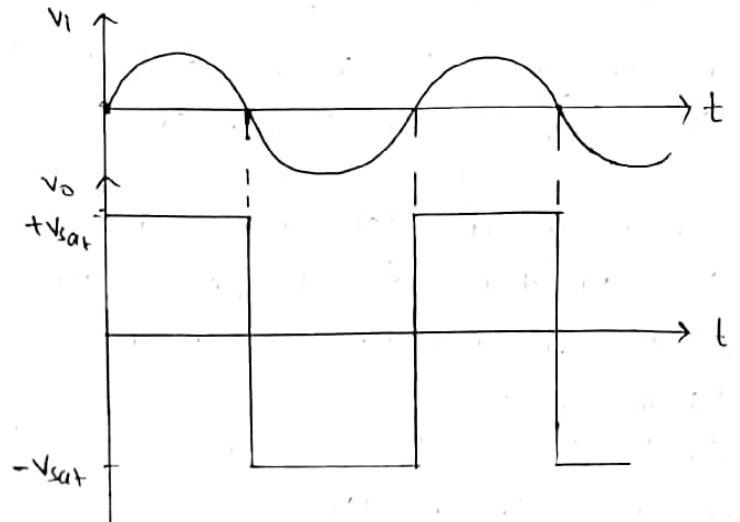The important application of comparator is zero crossing detector.

The types of ZCD are-

* Non-inverting ZCD
* Inverting ZCD
* Capacitor coupled ZCD.

Non-Inverting ZCD:

* If $V_i > 0 \Rightarrow V_0 = + V_{sat}$
* If $V_i < 0 \Rightarrow V_0 = - V_{sat}$

In a non-inverting zero crossing detector, the op-amp is used in open loop mode.
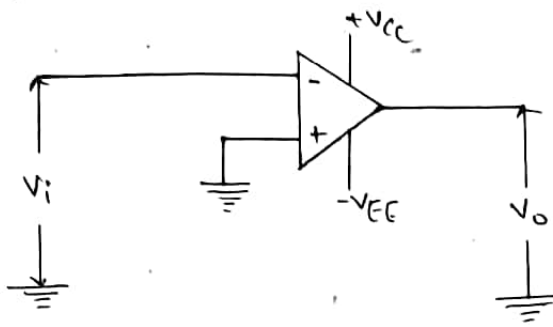
Inverting terminal is grounded and input is applied to the non-inverting terminal.

When the i/p is below ground level, the o/p is saturated at its -ve extreme. When the i/p goes above ground level by 300 uv, the o/p immediety switches to +ve saturation level.
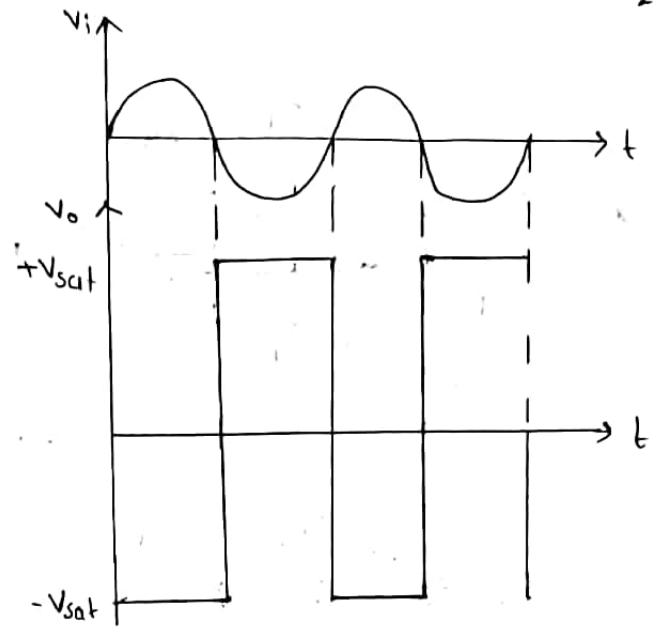
Each time the i/p voltage crosses zero level, the o/p switches from one saturation level to the other

Since, the o/p moves in a +ve direction when the i/p crosses zero from -ve to +ve, circuit is said to be non-inverting ZCD. Regardless of the i/p waveshape, the o/p is always a rectangular wave form.

Inverting ZCD

- If $V_i > 0 \Rightarrow V_0 = -V_{sat}$
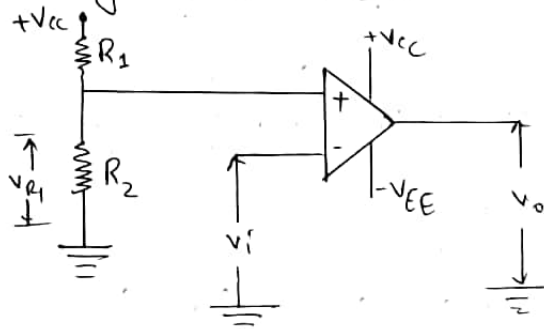- If $V_i < 0 \Rightarrow V_0 = +V_{sat}$

In inverting ZCD, the i/p is applied to the inverting i/p terminal while the non-inverting terminal is grounded.

When the i/p voltage crosses zero line going in +ve direction, the o/p goes -ve and vice-versa.

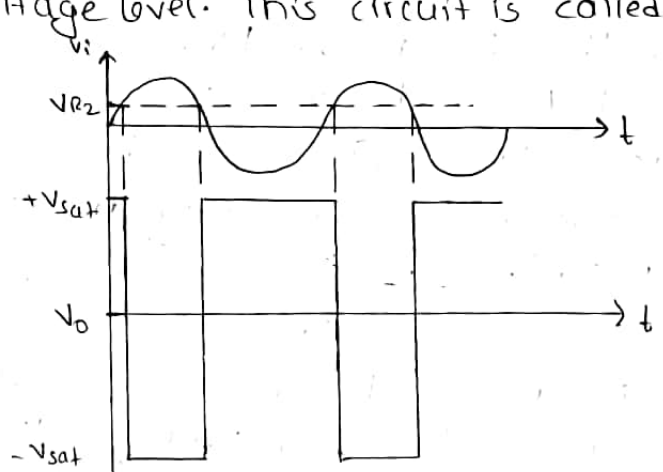This circuit is called as inverter.

Voltage Level detector:

Instead of being biased to ground level, the non-inverting i/p terminal of the op-amp could be biased to a +ve or -ve dc level as shown in fig. The circuit o/p changes when the i/p arrives at the bias voltage level. This circuit is called a voltage level detector.

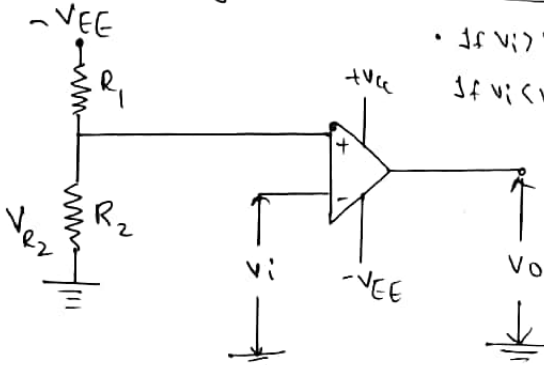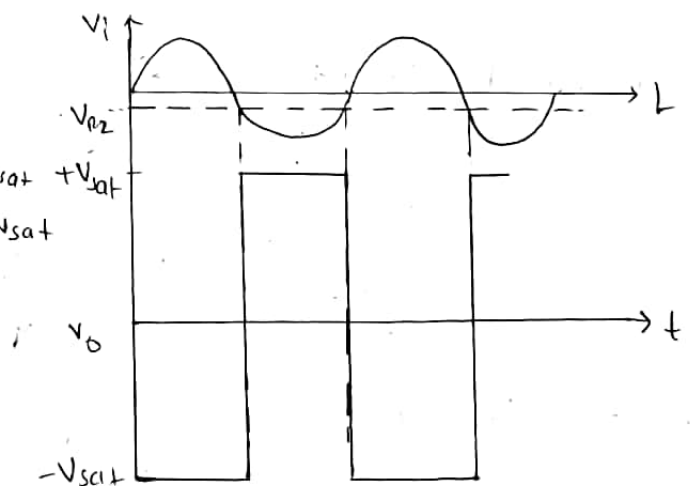(+ve voltage level detector)

If $V_i < V_{R2} \Rightarrow V_0 = +V_{sat}$
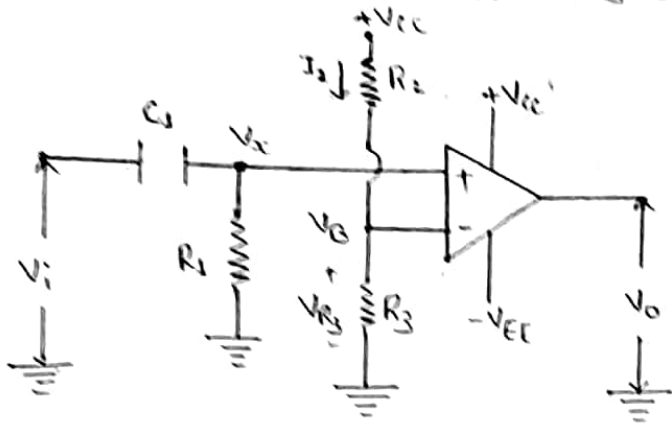
$V_i > V_{R2} \Rightarrow V_0 = -V_{sat}$

-ve voltage level detector

- If $V_i > V_{R2} \Rightarrow V_0 = -V_{sat} + V_{sat}$

If $V_i < V_{R2} \Rightarrow V_0 = +V_{sat}$

Capacitor coupled crossing detector:

- If $V_i < V_B \Rightarrow V_o = -V_{sat}$

  $V_i > V_B \Rightarrow V_o = +V_{sat}$

- $T = 2t$

  $t = T/2$

  $= \dfrac{1}{2f}$

The capacitor coupled crossing detector has the op-amp non-inv. input terminal connected to ground via resistor R_1, to provide a dc bias current path to op-amp.

Also, the inverting terminal is biased to a dc voltage level slightly above ground. This is required to ensure that the output is saturated in a -ve direction when no i/p is present.

The output switches to $+V_{sat}$ when the capacitor coupled signal drives the non inversting terminal above V_B and falls back to $-V_{sat}$ when the i/p drows below V_B.

Design:

* To design R_2 and R_3,

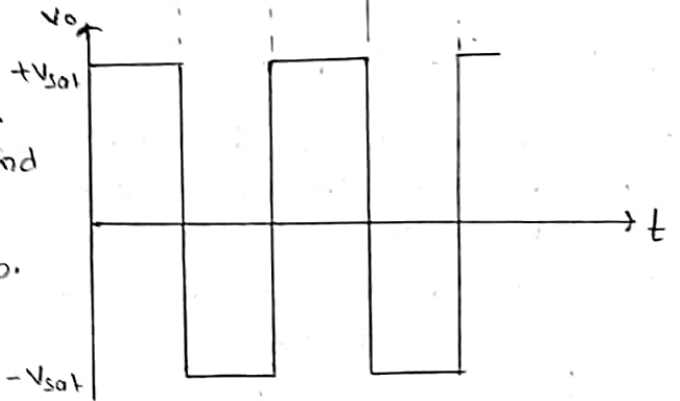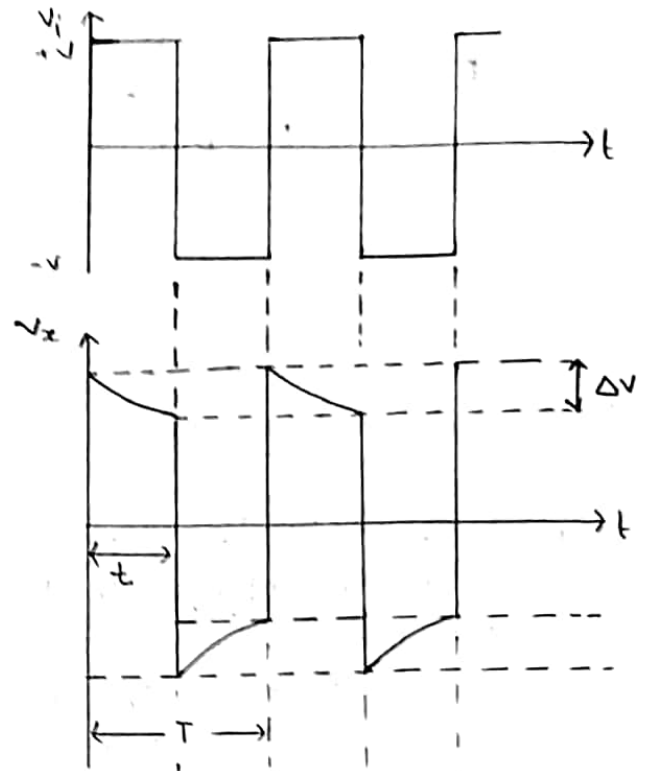 $I_2 = 100 \, I_{B\,max}$

  $V_B = 0.1V \quad [zero]$

  $V_{R2} = V_{cc} - V_B \qquad$ and $\quad V_{R3} = V_B$

  $R_2 = V_{R2} / I_2 \qquad\qquad\quad R_3 = V_{R3}/I_2$

* $R_1 = \dfrac{0.1 \, V_{BE}}{I_{B\,max}}$

✳ To find C_1.

- For <u>sinusoidal</u> input, to eliminate phase shift error which may make the circuit unstable., X_{C_1} must be smaller than R_1 at min. signal frequency f_1.

$$\therefore X_{C_1} = \frac{1}{20} R_1 \qquad \Rightarrow C_1 = \frac{1}{2\pi f_1 (R_1/20)}$$

- When a <u>square</u> wave is applied as an i/p to the capacitor coupled crossing detector, the waveform can develop tilt at op-amp input terminal as shown.
As long as the o/p is constant at saturation level, tilt is insignificant.
In such case, to determine C_1, first time t is measured for acceptable tilt in V_x.

$$I_1 = \frac{V_i}{R_1}$$

$$C_1 = \frac{I_1 t}{\Delta V} \qquad , \quad t = \frac{1}{2f}$$

For BIFIT

- Let, $R_2 = 1 M\Omega$
- Find I_2 & calculate R_3

$$R_2 = \frac{V_{R_2}}{I_2} = \frac{V_G - V_B}{I_2}$$

$$\therefore I_2 = \frac{V_{CC} - V_B}{R_2}$$

Find R_3, $R_3 = \frac{V_B}{I_2}$

- If V_i is <u>square wave</u>
Choose $C_1 = 0.1 uF$

$$C_1 = \frac{I_1 t}{\Delta V} \Rightarrow \text{Find } I_1 , \; \overset{w}{\Delta V} = 1v$$

$$I_1 = V_i/R_1$$

$$\therefore R_1 = V_i/I_1$$

- If V_i is sinusoidal wave

$$X_{C_1} = \frac{1}{20} R_1$$

Choose $C_1 = 0.1 uF$

Q. A capacitor coupled zero crossing detector is to handle 1 kHz square wave i/p with a peak to peak amplitude of 6V. Design a suitable circuit using a 741 op amp with a ±12V supply.

Sol^n: (Draw circuit diagram and waveform)

Let, $I_2 = 100 I_{B max}$

$$= 100 \times 500 nA$$

$$= 50 uA.$$

Let, $V_B = 0.1V$

$V_{R2} = V_{cc} - V_B = 12V - 0.1V = 11.9V$

- $R_2 = \dfrac{V_{R2}}{I_2} = \dfrac{11.9}{50 \times 10^{-6}} = 238 \, k\Omega \approx 220 \, k\Omega$

$V_{R3} = V_B = 0.1V$

- $R_3 = \dfrac{V_{R3}}{I_2} = \dfrac{0.1}{50 \times 10^{-6}} = 2 \, k\Omega \approx 1.8 \, k\Omega$

- $R_1 = \dfrac{0.1 V_{BE}}{I_{B\,max}} = \dfrac{0.1 \times 0.7}{500 \times 10^{-9}} = 140 \, k\Omega \approx 120 \, k\Omega$

$V_{i(peak)} = \dfrac{6V}{2} = 3V$

Square wave:

$I_1 = \dfrac{V_i}{R_1} = \dfrac{3}{120 \times 10^3} = 25 \, uA$

$t = \dfrac{1}{2f} = \dfrac{1}{2 \times 1 \times 10^3} = 500us$

$C_1 = \dfrac{I_1 t}{\Delta V} = \dfrac{25 \times 10^{-6} \times 500 \times 10^{-6}}{1} = 0.0125 \, uF \approx 0.015 \, uF$

8) A capacitor coupled ZCD is to provide an o/p voltage approx. $\pm 17V$ when a 3 kHz, with $\pm 2V$ square wave i/p is applied. Design a suitable detector using bipolar op amp.

Sol^n: $+V_{sat} = +17V$, $f = 3kHz$

$t = 1/2f = \dfrac{1}{2 \times 3 \times 10^3} = 0.167 \, ms$

$R_1 = \dfrac{0.1 V_{BE}}{I_{B\,max}} = \dfrac{0.1 \times 0.7}{500 \times 10^{-9}} = 140 \, k\Omega \approx 120 \, k\Omega$

$I_2 = 100 \, I_{B\,max} = 50 \, uA$

$R_2 = \dfrac{V_{cc} - V_B}{I_2} = \dfrac{18 - 0.1}{50 \times 10^{-6}} = 358 \, k\Omega \approx 330 \, k\Omega$

$R_3 = \dfrac{V_{R3}}{I_2} = \dfrac{V_B}{I_2} = \dfrac{0.1}{50 \times 10^{-6}} = 2 \, k\Omega \approx 1.8 \, k\Omega$

Sq. wave:

$C_1 = \dfrac{I_1 \Delta t}{\Delta V}$, $I_1 = \dfrac{V_i}{R_1} = \dfrac{2}{120 \times 10^3} = 16.67 \, uA$
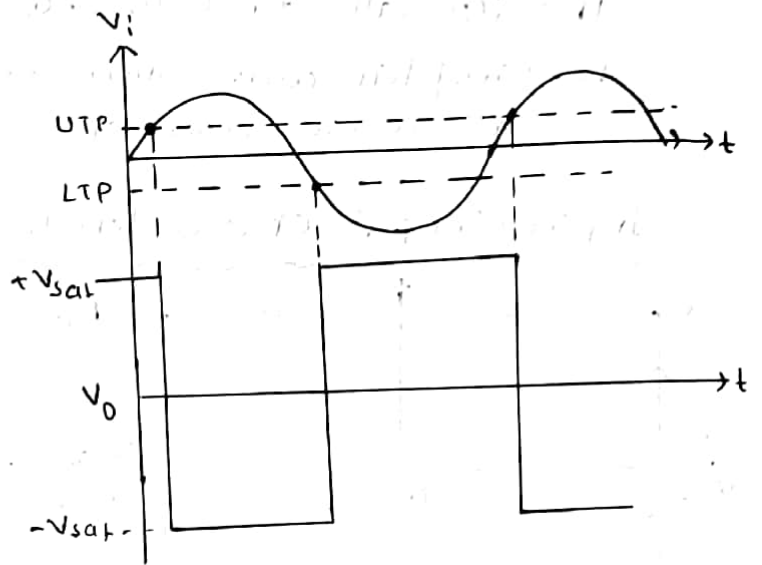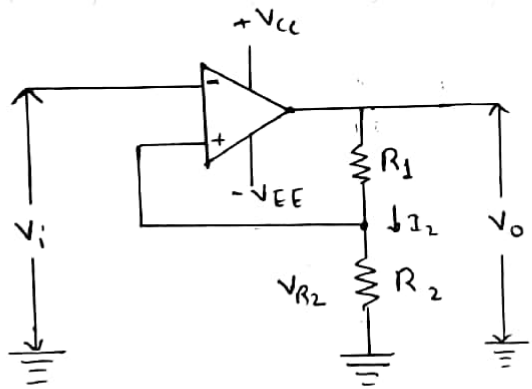
$= 2777.77 uF \approx 3000 \, uF$

BJFET: $R_2 = 1 M\Omega$

$I_2 = V_{R2}/R_2 = (V_{cc} - V_B)/R_2 = (18 - 0.1)/10^6 = 1.79 \times 10^{-5} A$

$R_3 = V_{R3}/I_2 = V_B/I_2 = 5.5 \, k\Omega \approx 5.6 \, k\Omega$

Choose, $C_1 = 0.1 uF$, $xc_1 = \dfrac{1}{2\pi f}$ $R_1 = 3.3 \, k\Omega$

Inverting schmitt Trigger circuit

In a basic comparator, a feed back is not used and the Op·Amp is used in the open loop mode. As open loop gain of Opamp is large, very small noise voltages can cause triggering of the comparator, to change its state. This may cause lot of problems in the applications of comparator as ZCD. Such unwanted noises cause the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called Regenerative comparator or schmitt trigger, which basically uses +ve feedback.

- $V_{R_2} = \dfrac{V_o}{(R_1 + R_2)} \times R_2$

- If $V_i < V_{R_2} \Rightarrow V_o = + V_{sat}$

  $V_{R_2} = \dfrac{+V_{sat}}{R_1 + R_2} \times R_2 \rightarrow$ UTP (Upper triggering point)

- If $V_i < V_{R_2} \Rightarrow V_o = - V_{sat}$

  $V_{R_2} = \dfrac{-V_{sat}}{R_1 + R_2} \times R_2 \rightarrow$ LTP (Lower triggering point)

The basic circuit of inverting schmitt trigger is shown above. The i/p is applied to the inverting terminal and +ve feedback is provided.

The voltage at non inverting i/p is $V_{R_2} = \dfrac{V_o}{R_1 + R_2} \times R_2$

when the o/p voltage is saturated in +ve direction at +V_{sat}, V_{R_2} is a positive quantity. When the o/p is at $-V_{sat}$, V_{R_2} is negative.
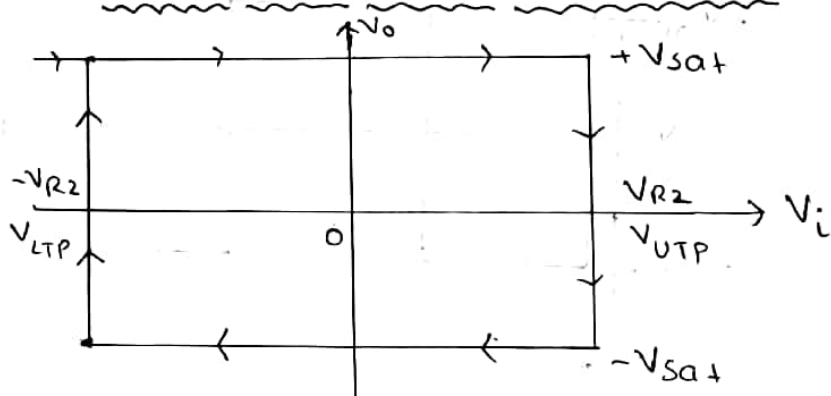
The o/p switch from the +ve saturation level to the -ve saturation level only when the inverting i/p terminal is raised above the voltage at non-inverting input terminal (V_{R2}).

$+V_{R2}$ is for +ve saturation when $V_0 = +V_{sat}$ and is called UTP (Upper Threshold point)

$-V_{R2}$ is for -ve saturation when $V_0 = -V_{sat}$ and is called LTP (Lower Threshold point)

The o/p switches from +ve to -ve when the i/p voltage reaches UTP and from -ve to +ve when the i/p falls to LTP. So, the o/p is always a rectangular waveform. So, it is also called sine to square wave converter.

Input/Output characteristics

Typical I/o characteristics of an op amp inverting schmitt trigger is shown above.

Initially with o/p at $+V_{sat}$ and i/p at zero, when V_i is raised to UTP, the o/p switches from $+V_{sat}$ to $-V_{sat}$. Any further increase in V_i above UTP maintains the o/p at $-V_{sat}$. When the i/p is being reduced from UTP to the LTP, the o/p remains at $-V_{sat}$.

When V_i equals the LTP, the o/p rapidally switches from $-V_{sat}$ to $+V_{sat}$. Now any further decrease in V_i below the LTP, maintains the o/p voltage at $+V_{sat}$.

The voltage difference between the upper and lower trigger points is referred to as <u>hysteresis</u>.

$$V_H = UTP - LTP$$

$$= \frac{+V_{sat}}{R_1 + R_2} \times R_2 - \left[\frac{-V_{sat}}{R_1 + R_2} \times R_2 \right]$$

When $V_i < LTP$, $V_0 = +V_{sat}$

$V_i > UTP$, $V_0 = -V_{sat}$

- $V_i < UTP \Rightarrow V_0 = +V_{sat}$
- $V_i > UTP \Rightarrow V_0 = -V_{sat}$
- $V_i < LTP \Rightarrow V_0 = -V_{sat}$
- $V_i > LTP \Rightarrow V_0 = +V_{sat}$

$LTP < V_i < UTP \Rightarrow V_0 = $ Previous state.

Design steps :

Let, the current through R_1 and R_2 is I_2.

- $I_2 = 100 \, I_{B\,max}$
- $R_2 = \dfrac{\text{Triggering voltage}}{I_2}$
- $R_1 = \dfrac{V_0 - \text{Triggering voltage}}{I_2}$

BIFET :

- choose $R_1 = 1 \, m\Omega$
- Find I_2

$$I_2 = \frac{V_0 - \text{Triggering voltage}}{R_1}$$

$\Rightarrow$ Find R_2

$$R_2 = \frac{\text{Triggering voltage}}{I_2}$$

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8. Using a 741 Op amp with a supply of $\pm 12V$, design an inverting schmitt trigger circuit to have a trigger point of $\pm 2V$

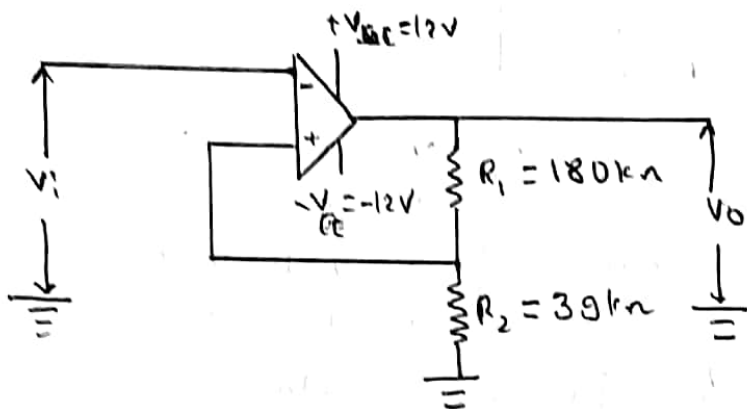Soln: Let, $I_2 = 100 \, I_{B\,max}$

$$= 50 \, uA$$

$$+V_{R_2} = UTP = 2V$$

$$R_2 = \frac{V_{R_2}}{I_2} = \frac{2V}{50 \, uA} = 40 \, k\Omega \approx 39 \, k\Omega$$

$$V_{R1} = V_{0_{sat}} - V_{R2} = (12-1) - 2 = 9V$$

$$R_3 = \frac{V_{R1}}{I_2} = 180 \, k\Omega \simeq 180 \, k\Omega$$

BIFET

$$R_3 = 1 M\Omega$$

$$I_2 = \frac{V_0 - Triggering \, voltage}{R_1} = \frac{11 - 2}{1 \times 10^6} = 9 \, uA$$

$$R_2 = \frac{Triggering \, voltage}{I_2} = \frac{2}{9 \times 10^6} = 222 \, k\Omega \approx 220 \, k\Omega$$

Q. An inverting schmitt trigger is to be designed with triggering voltage $\pm 0.5V$ and to produce the o/p = $\pm 11V$. Use 741 op Amp.

$Soln$: $I_2 = 100 \, I_{Bmax} = 50 \, uA$

$$R_2 = \frac{Triggering \, voltage}{I_2} = \frac{0.5}{50 \times 10^6} = 10 \, k\Omega$$

$$R_1 = \frac{11 - 0.5}{50 \times 10^{-6}} = 210 \approx 180 \, k\Omega$$

Q. Design an inv. schmitt trigger to have triggering points of $\pm 4V$ with a supply of $\pm 15V$

$Soln$: $I_2 = 100 \, I_{Bmax} = 50 \, uA$

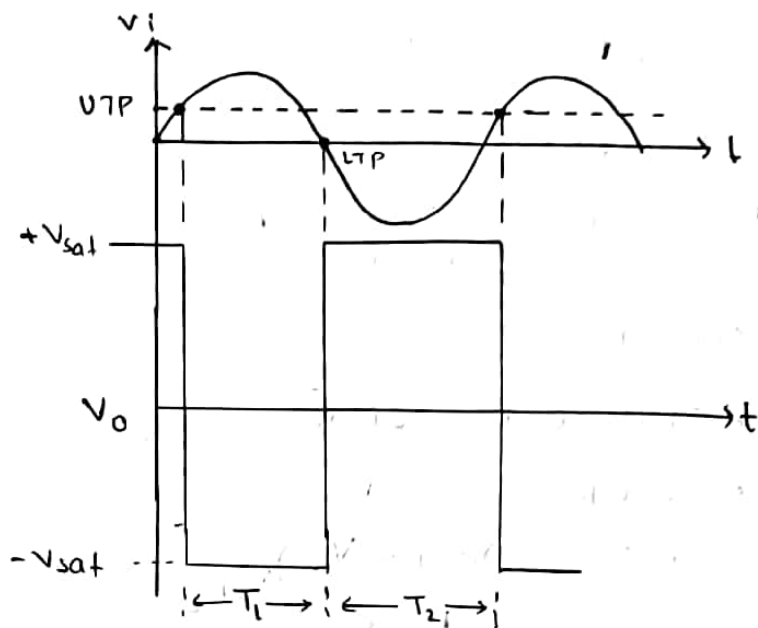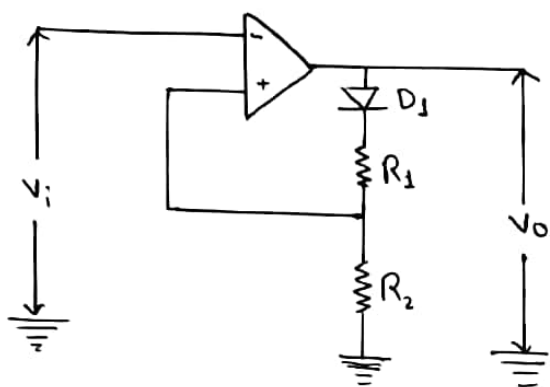$$R_2 = \frac{4}{50 \times 10^6} = 80 \, k\Omega$$

$$R_1 = \frac{14 - 4}{50 \times 10^{-6}} = 200 \, k\Omega$$

Adjusting Triggering points

Inverting schmitt trigger circuits with different UTP & LTP

Asymmetrical schmitt Trigger

a)

- If $V_i < V_{R2}$, $V_o = +V_{sat}$

  D1 is F.B , $V_{R2} = UTP$

- $V_{R2} = UTP = \left(\dfrac{+V_{sat} - V_F}{R_1 + R_2}\right) \times R_2$

  $V_F \rightarrow$ Diode voltage.

- If $V_i > V_{R2}$, $V_o = -V_{sat}$

  D1 is R.B , $V_{R2} = 0$ (LTP)

$T_1 \ll T_2 \rightarrow$ Asymmetrical

In the above circuit, UTP is combined with a zero voltage LTP. When the o/p is +ve, D1 is Forward·biased and UTP is the $^{vtg}\wedge$ drop across R2. When the o/p is -ve, D1 is reverse biased, only the op-amp input bias current flows in R2 and the op'amp non-inverting i/p terminal is held close to ground level. The o/p will go +ve once again when the i/p voltage is reduced below ground level.

The diode D1 must be selected to have a maximum reverse voltage greater than the circuit supply voltage. It's maximum reverse recovery time (t_{rr}) should be much smaller than the min pulse width of the i/p signal.

$$\therefore \quad t_{rr} \leq \frac{\text{Min. pulse width}}{10}$$

Design:

741:

Let, $I_2 = 500 \mu A$ (To handle diode forward current, $I_2 = 500 \mu A$)
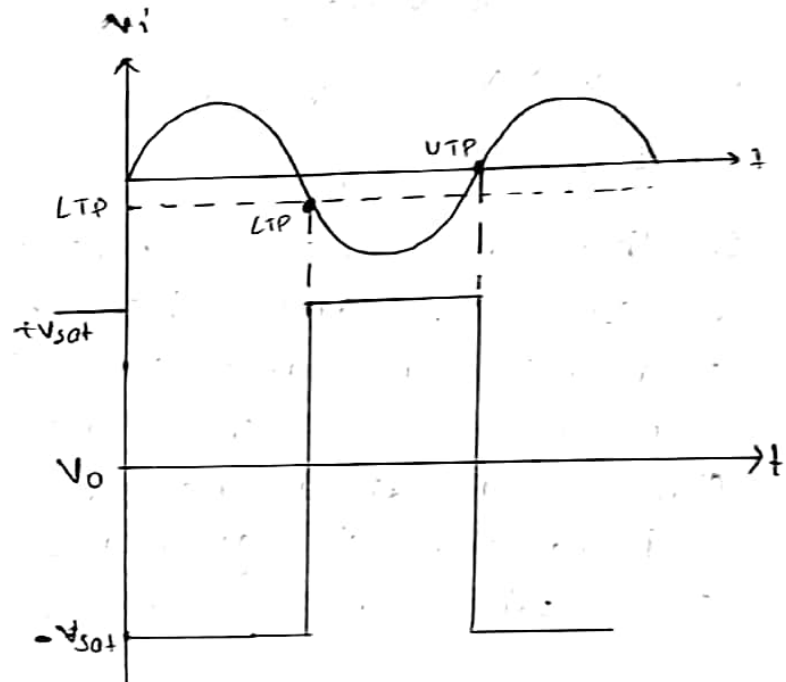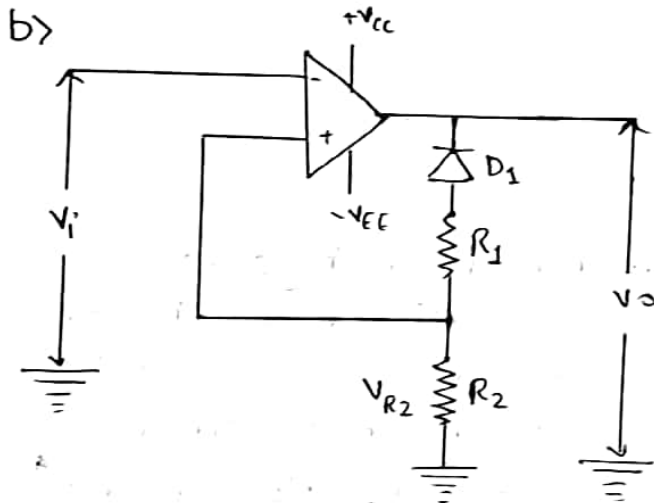
- $R_2 = \dfrac{UTP}{I_2}$

- To find R_1,
  $$UTP = \left(\dfrac{+Vsat - V_F}{R_1 + R_2}\right) R_2$$

BIFET:

- choose $R_1 = 1M\Omega$

- Find R_2.
  $$UTP = \dfrac{(+Vsat - V_F)}{R_1 + R_2} \times R_2$$

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b)

- If $V_i > V_{R2}$, $V_0 = -Vsat$

  D_1 is F.B, $V_{R2} = LTP$

  $$-V_{R2} = \dfrac{(-Vsat + V_F)}{R_1 + R_2} \times R_2$$

- If $V_i < V_{R2}$, $V_0 = + Vsat$

  D_1 is R.B, $V_{R2} = 0$

Design:

$I_2 = 500 \mu A$

$R_2 = \dfrac{LTP}{I_2}$

Find R_1

Q. An inverting schmitt trigger is to have UTP = 1V and LTP = 0V. Design a suitable circuit using bipolar op amp with supply voltage of, ±15V.

Soln: $I_2 = 500 \mu A$

$$R_2 = \frac{UTP}{I_2} = \frac{1}{500 \times 10^6} = 2 k\Omega \quad \simeq 1.8 k\Omega$$

To find R_1,

$$UTP = \frac{(14 - 0.7)}{R_1 + R_2} \times R_2$$

$$\Rightarrow 1 = \frac{(14 - 0.7)}{(R_1 + 1.8 \times 10^3)} \times 1.8 \times 10^3$$

$$\Rightarrow R_1 = (14 - 0.7) \times 1.8 \times 10^3 - 1.8 \times 10^3$$

$$= 22.14 k\Omega$$

Q. Design a suitable circuit with UTP = 0V and LTP = 2.5V with power supply ±18V. Use 741 op Amp.
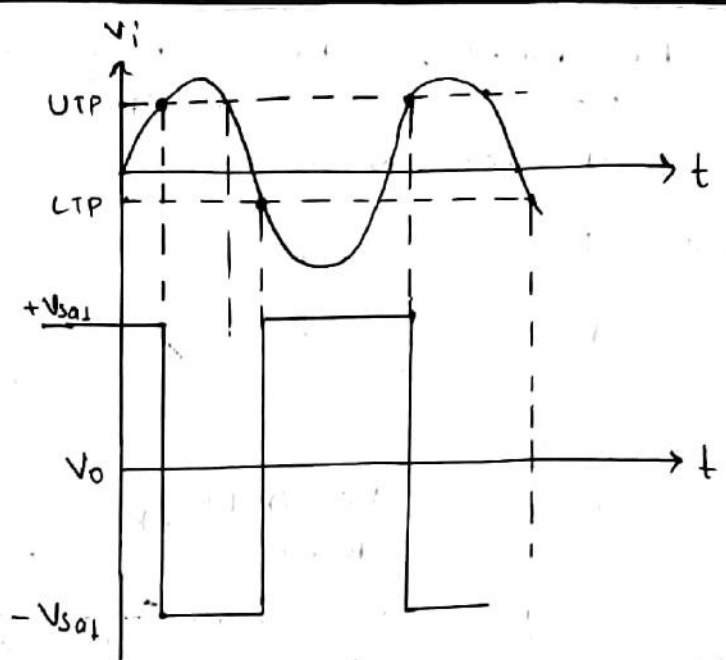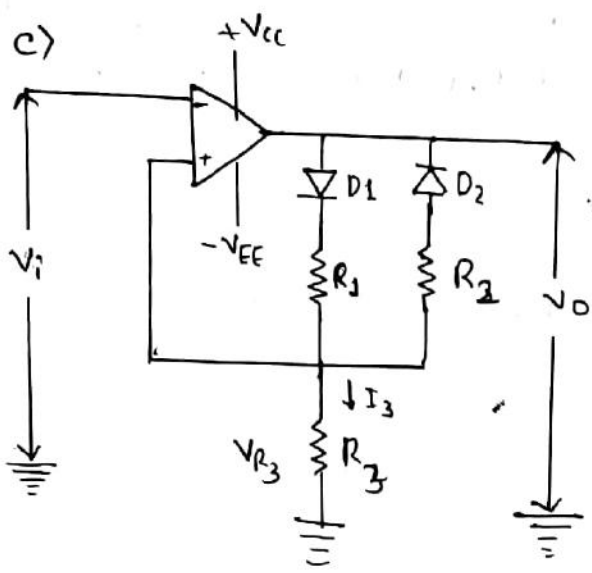
Soln: $I_2 = 500 \mu A$

$$R_2 = \frac{LTP}{I_2} = \frac{2.5}{500 \times 10^6} = 5 k\Omega \simeq 4.7 k\Omega$$

To find R_1,

$$LTP = \left(\frac{-V_{sat} + V_f}{R_1 + R_2} \right) \times R_2$$

$$\Rightarrow -2.5 = \frac{(-17 + 0.7)}{R_1 + 4.7 \times 10^3} \times 4.7 \times 10^3$$

$$\Rightarrow R_1 = 25.84 k\Omega$$

$$\simeq 22 k\Omega$$

c)

The above circuit has two different level trigger points.

- If $V_i < V_{R3} \Rightarrow V_0 = +V_{sat}$

  D1 is F.B and D2 is R.B

  $$V_{R3} = UTP = \frac{(+V_{sat} - V_F)}{R_1 + R_3} \times R_3 \quad , \quad \text{where } V_F \text{ is forward voltage drop of D1}$$

- If $V_i > V_{R3} \Rightarrow V_0 = -V_{sat}$

  D1 is R.B and D2 is F.B

  $$V_{R3} = LTP = \frac{(-V_{sat} + V_F)}{R_2 + R_3} \times R_3$$

Design: Choose $I_3 = 500 \mu A$

$$R_3 = \frac{UTP}{I_3}$$

To find R_1 : $UTP = \frac{(+V_{sat} - V_F)}{R_1 + R_3} \times R_3$

To find R_2 : $LTP = \frac{(-V_{sat} + V_F)}{R_2 + R_3} \times R_3$

θ. Design an Inv. schmitt trigger with UTP=1.5v & LTP=-3v, with ±18v supply using bipolar op amp.

Soln: $I_3 = 500 \mu A$

$$R_3 = \frac{1.5}{500 \times 10^{-6}} = 3k\Omega \approx 2.7 k\Omega$$

$$UTP = \left(\frac{+V_{sat} - V_F}{R_1 + R_3}\right) R_3 \Rightarrow R_1 = 26.69k\Omega \approx 27 k\Omega$$

$$LTP = \left(\frac{-V_{sat} + V_F}{R_2 + R_3}\right) \times R_3 \Rightarrow R_2 = 11.97 k\Omega \approx 12 k\Omega$$

'Multivibrators using Op Amp'

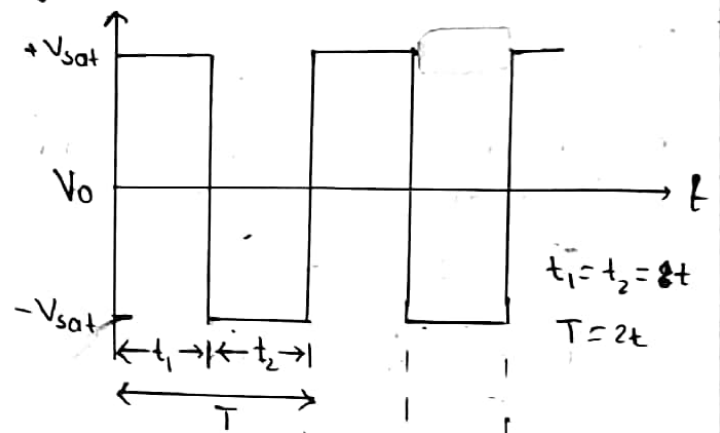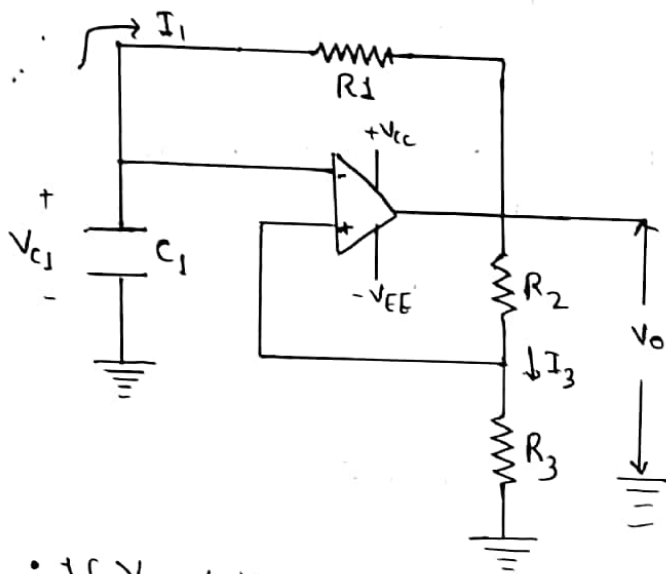Multivibrators are regenerative circuits that are used commonly in timing applications.

There are two types:-

i) astable multivibrator   ii) Monostable multivibrator.

i) Astable Multivibrator using Op Amp

An astable mv is a circuit that is continuously switching its o/p voltage between high and low levels. It has no stable state.

It is also called a free running multivibrator

$$\text{If } V_{C_1} < V_{R3} \Rightarrow V_0 = + V_{sat}$$

$$UTP \, (V_{R3}) = \frac{+ V_{sat}}{R_2 + R_3} \times R_3$$

$$\text{If } V_{C_1} > V_{R3} \Rightarrow V_0 = - V_{sat}$$

$$LTP \, (-V_{R3}) = \frac{- V_{sat}}{R_2 + R_3} \times R_3$$

The circuit diagram of Amv using schmitt trigger is shown in figure. The op-amp with resistors R_2 and R_3 forms an inverting schmitt trigger circuit. The i/p voltage to schmitt trigger is the voltage across capacitor C_1 which is charged from the op-amp o/p via resistor R_1.

When the power is turned ON, the output automatically swing either to $+V_{sat}$ or to $-V_{sat}$. Since, these are the only stable states allowed by the schmitt trigger.
Let, the circuit o/p be at +ve saturation level, current flows into the capacitor, charging it until the V_{c1} reaches the UTP of the schmitt trigger.
The o/p then rapidly switches to the -ve saturation level. Now, capacitor starts discharging via R_1 and capacitor charges with opposite polarity. This continues until V_{c1} reaches LTP, then the o/p rapidly switches back to +ve saturation level, and cycle starts again.

Design:

- The minimum current through R_1 is selected to be much larger than the op-amp input bias current

  $$I_1 = 100 \, I_{B\,max}$$

- $$R_1 = \frac{|V_0| - UTP}{I_1}$$

- Once R_1 is determined, C_1 can be calculated from the capacitor charging equation.

  If schmitt trigger UTP and LTP are selected to be much smaller than op-amp o/p voltage, the voltage across R_1 will not change much.
  Consequently, the capacitor charging current (I_1) can be a constant & from which C_1 can be obtained.

  $$C_1 = \frac{I_1 \times t}{\Delta V} \quad , \quad \Delta V = UTP - LTP \qquad UTP = +0.5V$$
  $$= 1V \qquad LTP = -0.5V$$

- Let, $I_3 = 100 \, I_{B\,max}$
- $R_3 = \dfrac{UTP}{I_3}$
- $R_2 = \dfrac{|V_0| - UTP}{I_3}$

BIFET

The capacitance of C_1 should be first selected to be much larger than stray capacitance.

- Choose $C_1 = 0.1 \, \mu F$.

- Find I_1, $\quad I_1 = \dfrac{C_1 \, \Delta V}{t_1}$

- $R_1 = \dfrac{|V_0| - UTP}{I_1}$

- Choose $R_2 = 1 M\Omega$

- Find I_3, $\quad I_3 = \dfrac{|V_0| - UTP}{R_2}$

- $R_3 = \dfrac{UTP}{I_3}$

Q. Using a BIFET op amp, design an Amv to have a $\pm 9V$ o/p with frequency of $1 kHz$.

Soln: For $V_0 = \pm 9v$

$$V_{cc} = \pm V_0 + 1 = \pm 9v + 1 = \pm 10v$$

select, $UTP = LTP = 0.5 \, V$

Let, $R_2 = 1 M\Omega$

$$I_3 = \dfrac{|V_0| - UTP}{R_2} = \dfrac{9v - 0.5v}{1 M\Omega} = 8.5 \mu A$$

$$R_3 = \dfrac{UTP}{I_3} = \dfrac{0.5 \, V}{8.5 \mu A} = 59 k\Omega \quad \approx 56 \, k\Omega$$

Let, $C_1 = 0.1 \, \mu F$

$$t_1 = \dfrac{1}{2f} = \dfrac{1}{2 \times 10^3} = 500 \mu s$$

$$I_1 = \dfrac{C_1 \, \Delta v}{t} = 200 \mu A$$

$$R_1 = \dfrac{V_0 - UTP}{I_1} = 42.5 \, k\Omega \quad \approx 39 \, k\Omega$$

Q. Design an OpAmp Amv to have an o/p frequency of 400 Hz. Use a 741 Op Amp with a supply of $\pm 18v$.

Sol^n:

$f = 400 Hz, \quad T = 2.5ms, \quad t_1 = 1.25ms$

Let, $I_1 = 100 \, I_{Bmax} = 50 \, uA$

$$R_1 = \frac{17 - 0.5}{50 \times 10^{-6}} = 330 \, k\Omega$$

$$C_1 = \frac{I_1 t}{\Delta v} = \frac{50 \times 10^{-6} \times 1.25 \times 10^{-3}}{1} = 62.5 nF \approx 0.064 uF$$

$$I_3 = 100 \, I_{Bmax} = 50 uA$$

$$R_3 = \frac{0.5}{50 \times 10^{-6}} = 10 k\Omega$$

$$R_2 = \frac{17 - 0.5}{50 \times 10^{-6}} = 330 k\Omega$$

BIFET

$R_2 = 1 M\Omega$

$$I_3 = \frac{|V_0| - UTP}{R_2} = \frac{17 - 0.5}{1 \times 10^{6}} = 16.5 uA$$

$$R_3 = \frac{UTP}{I_3} = \frac{0.5}{16.5 \times 10^{-6}} = 30.3 k\Omega$$

$C_1 = 0.1 uF$

$$t = \frac{1}{2f} = \frac{1}{2 \times 400} = \frac{1}{800} = 1.25 mA$$

$$I_1 = \frac{C_1 \, \Delta v}{t} = \frac{0.1 \times 10^{-6}}{1.25 \times 10^{-3}} = 80 uA$$

$$R_1 = \frac{V_0 - UTP}{I_1} = \frac{17 - 0.5}{80 \times 10^{-6}} = 206.25 k\Omega$$

Q. Design Amv using 741 with $\pm 15V$ supply with $t_{on} = t_{off} = 1ms$.

Sol^n:

$I_1 = 100 \, I_{Bmax} = 50 uA$

$$R_1 = \frac{14 - 0.5}{50 \times 10^{-6}} = 270 k\Omega$$

$$C_1 = \frac{I_1 t_1}{\Delta v} = 50 \times 10^{-6} \times 10^{-3} = 0.05 uF$$

$$I_3 = 100 \, I_{Bmax} = 50 uA$$
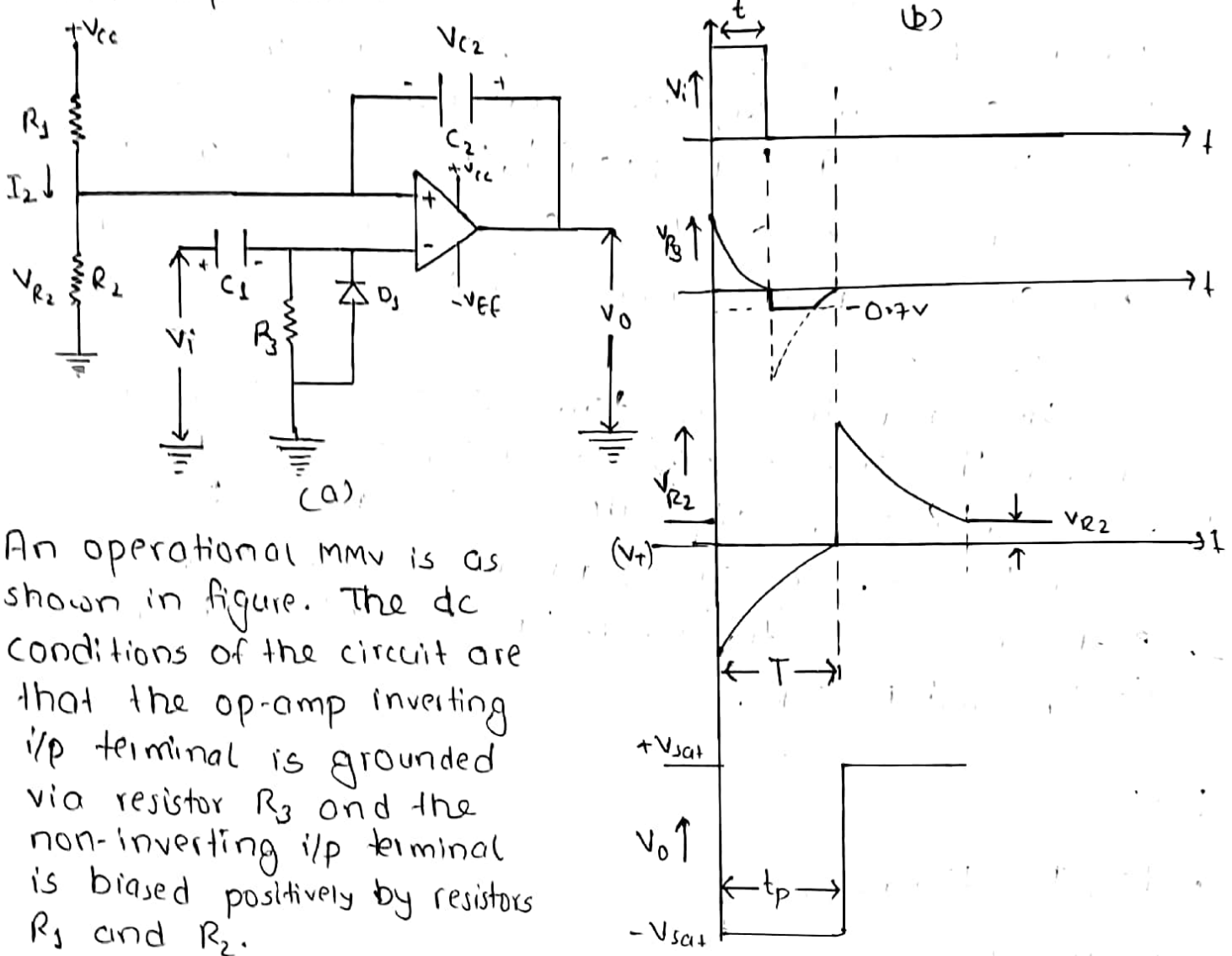
$$R_3 = 0.5 / (50 \times 10^{-6}) = 10 k\Omega$$

$$R_2 = \frac{14 - 0.5}{50 \times 10^{-6}} = 270 k\Omega$$

Monostable Multivibrator

A MMV has one stable output state. Its normal o/p voltage may be low or high and it stays in the normal state until it is triggered. When a trigger i/p is applied, the output switches to its opposite state for a time dependent on the circuit components.

(a)

(b)

An operational MMV is as shown in figure. The dc conditions of the circuit are that the op-amp inverting i/p terminal is grounded via resistor R_3 and the non-inverting i/p terminal is biased positively by resistors R_1 and R_2.

Consequently, the op-amp is normally at +ve saturation & capacitor C_2 is charged with the polarity shown.

An input pulse V_i applied to C_1 is differentiated by R_3 & C_1 to produce positive and -ve spikes (V_{R_3}) at the op-amp inverting i/p terminal as shown in figure (b).

The -ve spike is clipped at -0.7v by diode D_1 so that it has no effect on the circuit.

The positive spike lips the inverting input terminal above the bias level of the non-inverting input and thus causes the

op-amp o/p to switch to the -ve saturation level. The spike has a short time duration, so the inverting input terminal quickly returns to zero voltage level.

However, when i/p goes to $-V_{sat}$, the charge on C_2 drives the non-inverting input voltage (V_T) down to

$$V_+ = -V_{sat} - V_{C_2}$$

which is below the ground level. And this voltage is present at non-inverting i/p terminal even after the input triggering spike has disappeared, thus keeping o/p at $-V_{sat}$.

With the o/p at $-V_{sat}$, C_2 discharges via R_1 & R_2, thus gradually raising non-inverting i/p terminal towards ground level.

When non-inverting terminal goes slightly above ground, the op-amp o/p immedietly switches back to $+V_{sat}$ once again and the circuit is returned to its original state. The circuit produces a -ve going pulse each time it is triggered. The pw of o/p depends on C_2, V_{R_2} and R_1 & R_2.

Design:

- Let, $I_2 = 100 I_{B max}$

- Assume, $V_{R_2} = 0.5 V$

- $R_2 = \dfrac{V_{R_2}}{I_2}$ and $R_1 = \dfrac{+V_{cc} - V_{R_2}}{I_2}$

- $R_3' = R_{max} = \dfrac{0.1 V_{BE}}{I_{B max}}$

- To generate spikes from i/p pulse, the time constant $C_1 R_3$ should be approximately one-tenth of i/p pulse width.

  $C_1 R_3 = 0.1 t$

  $\Rightarrow C_1 = \dfrac{0.1 t}{R_3}$

or, c_1 might be selected first much larger than stray capacitance, then R_3 can be calculated from the above equation.

- To find c_2,

consider the capacitor charging equation

$$e_c = E - [E-E_0] e^{-t_p/RC}$$

$$\Rightarrow e^{t_p/RC} = \frac{E-e_c}{(E-E_0)}$$

$$-t_p/RC = \ln\left(\frac{E-e_c}{E-E_0}\right).$$

$$t_p = RC \ln\left[\frac{E-E_0}{E-e_c}\right]$$

At $t = p_w$, $C = C_2$ & $R = R_1 \| R_2$

$$t_p = (R_1 \| R_2) C_2 \ln\left[\frac{E-E_0}{E-e_c}\right]$$

- $$C_2 = \frac{t_p}{(R_1 \| R_2) \ln\left[\frac{E-E_0}{E-e_c}\right]}$$

$t_p \rightarrow$ pulse width (pw)

- $E \rightarrow$ Capacitor charging voltage that is the voltage that it would charge to after triggering if it were allowed to continue charging without the o/p switching from $-V_{sat}$.

$$\therefore E = V_{R_2} - (-V_{sat})$$

- $E_0 \rightarrow E_0$ is the initial capacitor voltage before triggering

Taking E as a +ve quantity, E_0 must be assigned a -ve polarity.

$$E_0 = -[+V_{sat} - V_{R_2}] = V_{R_2} - (+V_{sat})$$

$e_c \rightarrow e_c$ is the final capacitor voltage at which op-amp output switches from $-V_{sat}$ to $+V_{sat}$. This is the voltage across C_2 when the non-inverting i/p terminal is at ground level and the o/p is still at $-V_{sat}$.

$\therefore e_c = 0 - (-V_{sat})$

$e_c = + V_{sat}$

~~~~ x ~~~~

Q. Design a MMV to have on o/p pulse width of 1ms when triggered by a 2v, 100 us input pulse. Use 741 op amp with $\pm$ 12v supply.

$\underline{soln:}$ Let, $I_2 = 100 \; I_{B \, max} = 50 uA$

Let, $V_{R2} < V_1$

$V_{R2} = 0.5 V$

$R_2 = \dfrac{V_{R2}}{I_2} = 10 k\Omega \; (std \; value)$

$R_1 = \dfrac{V_{cc} - V_{R2}}{I_2} = 230 k\Omega \approx 220 k\Omega$

$E = V_{R2} - [-V_{sat}] \approx 0.5 - [-12+1]$

$\quad \approx -10.5 V$

$e_c = +V_{sat} = (12-1) = 11 V$

$C_2 = \dfrac{t_p}{(R_1 \| R_2) \ln\left(\dfrac{E-0}{E-e_c}\right)} = 0.027 uF \approx 0.03 uF$

$R_3 (max) = 140 k\Omega \approx 120 k\Omega$

$C_1 = \dfrac{0.1t}{R_3} = \dfrac{0.1 \times 100 \times 10^{-6}}{120 \times 10^3} = 83 pF \approx 91 pF$

Precision Half-wave circuits

* ## Saturating precision Rectifier

The circuit of an op-amp precision rectifier is shown in fig. It is simply a voltage follower with a diode connected between the op-amp o/p terminal and the circuit output point.
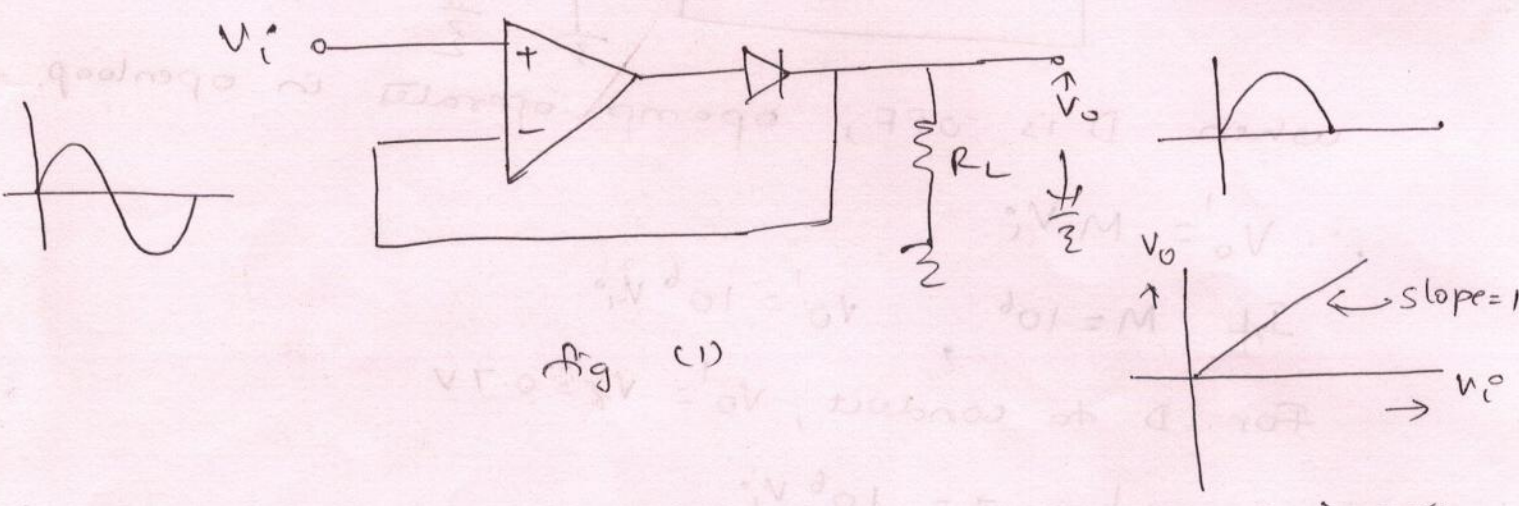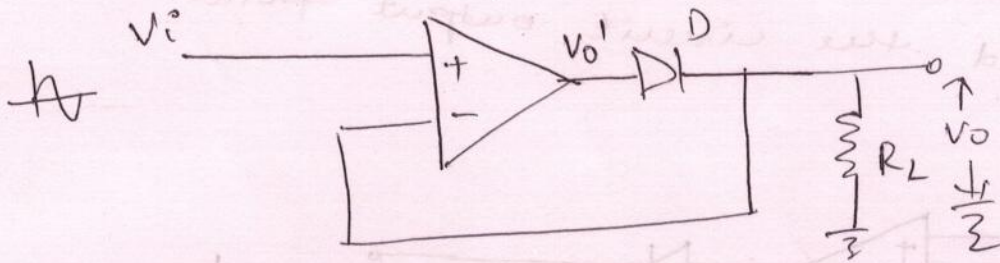

Fig (1)

Case (i): During positive Half-cycle, Diode D_1 is off. The feedback path is broken. The current through R_L is zero. ∴ $V_0 = 0$.

Case (i): During positive Half-cycle Diode D_1 is ON. and op-amp circuit acts as voltage follower.
∴ $V_0 = V_i$

Case (ii): During negative half cycle D_1 is OFF. The feedback path is broken. The current through R_L is zero. ∴ $V_0 = 0$.

NOTE:- Ordinary Rectifiers using Si diodes have a cut-in voltage of 0.7V. Hence the Rectification of Sinusoidal Signal starts above only above the cut-in Voltage V_γ. Below V_γ rectification is not possible. In precision Rectifier, rectification below V_γ is possible.

when D is OFF, opamp operates in openloop.

$$\therefore V_0' = M V_i$$

If $M = 10^6$, $\quad V_0' = 10^6 V_i$

For D to conduct, $V_0' = V_\gamma = 0.7V$

$$\therefore V_0' = 0.7 = 10^6 V_i$$

$$V_i = 0.7 \, \mu V \simeq 0$$

$\therefore$ Rectification starts almost down to 0V.

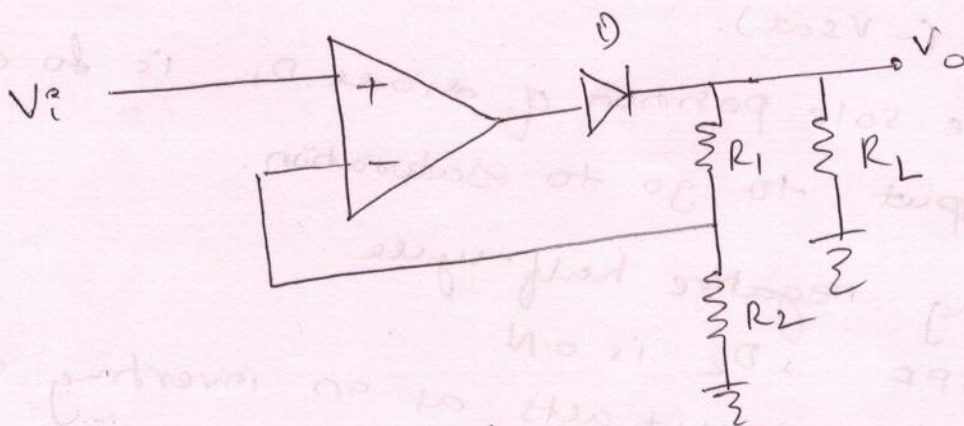By reversing the polarity of the diode it is possible to rectify the negative half-cycle.

Advantages of precision Rectifier over ordinary Rectifier

1. No diode drop between input and output.
2. Rectification is possible below V_γ.
3. Amplification is possible.
4. Low output impedance. ie it behaves as an ideal diode.

In the above fig, during negative half-cycle diode D is OFF, and op-amp operates in open loop. Open loop voltage gain of opamp is very high and output of opamp goes to $-V_{sat}$. This limits the frequency response of the circuit. For high frequency application, a non-saturating precision rectifier must be used.

The fig below shows the precision rectifier with voltage gain. This is a non-inverting amplifier with diode included. The circuit is designed as non-inverting amplifier. The current through R_1 and R_2 should be a minimum of $100 \mu A$ to ensure diode is operating correctly. A minimum of $500 \mu A$ is a good design.
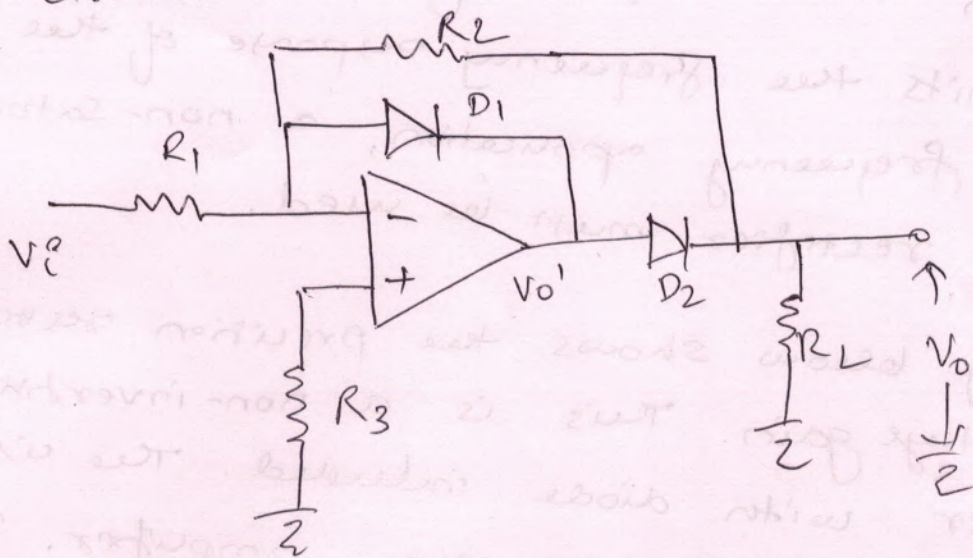

(b)

when D is ON,
$$V_0 = \left(1 + \frac{R_1}{R_2}\right) V_i$$

A Non-saturating precision Rectifier

Fig below shows inverting precision half-wave rectifier, where the o/p of opamp is not driven into saturation.

Case (i) During positive half-cycle

D_1 is ON, D_2 is OFF, $V_0 = 0$.

Inverting terminal being at virtual ground, V_0' is clamped to $-0.7V$ and does not reach saturation $(-V_{sat})$.

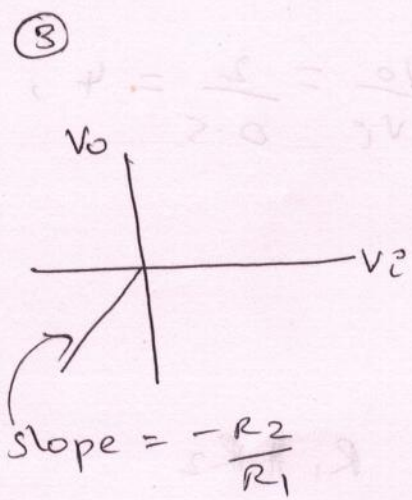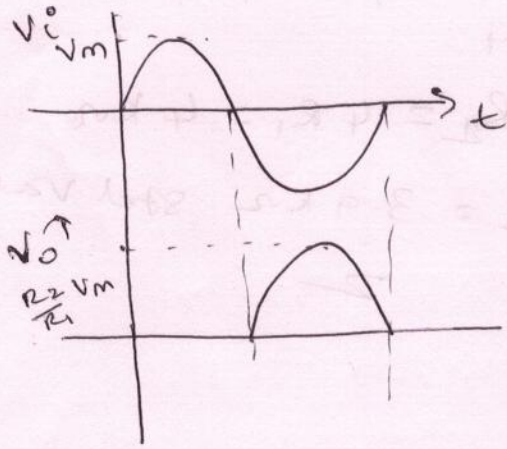The sole position of diode D_1 is to avoid opamp output to go to saturation.

Case (ii) During negative half-cycle

D_1 is OFF, D_2 is ON

The opamp circuit acts as an inverting amplifier

$$\therefore V_0 = -\frac{R_2 V_i}{R_1}$$

If $R_1 = R_2$

$V_0 = -V_i$, If $R_2 > R_1$, the o/p is amplified.

If the polarities of D_1 and D_2 are reversed, positive half cycle will be rectified with inversion and negative half cycle is clipped.

Design

The inverting amplifier is designed first. The reverse break down voltage of diode must be greater than the supply voltage. The diode reverse recovery time must be much smaller than the time periods of the highest signal frequency to be processed.

Ex:- Design a Non-saturating precision HWR as shown above to produce a 2V peak output from a sine wave i/p with a peak value of 0.5V and frequency of 1MHz. Use a bipolar op-amp. with a supply of ±15V.

let $I_1 \gg I_{B\,max}$

$\therefore I_1 = 500\mu A$

$\therefore R_1 = \dfrac{V_i}{I_1} = \dfrac{0.5m}{500 \times 10^{-6}} = 1k\Omega$

$$R_1 \approx 1k\Omega$$

Gain $\dfrac{V_o}{V_i} = \dfrac{2}{0.5} = 4$, $\qquad \dfrac{R_2}{R_1} = 4$

$\qquad\qquad\qquad\qquad \therefore R_2 = 4R_1 = 4k\Omega$

$\qquad\qquad\qquad\qquad R_2 = 3.9 k\Omega$ std value

$R_3 = R_1 \,\#\, R_2$

$\qquad = 1k \,\|\, 3.9k = 796\Omega$

$\qquad$ we $R_3 = 820\,\Omega$

The breakdown voltage of D_1 and D_2

should be $\gg 30V$ $(15 - (-15V))$

$\qquad t_{rr} < T$, $\qquad T = \dfrac{1}{10^6} = 1\mu s$

$\qquad$ let $t_{rr} = \dfrac{T}{10} = 0.1\mu s$

Two output precision Rectifier

The fig below shows two output precision

Half-wave rectifier.

Case (i)   During positive half-cycle

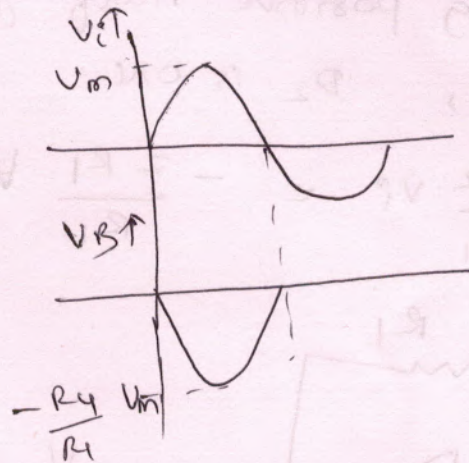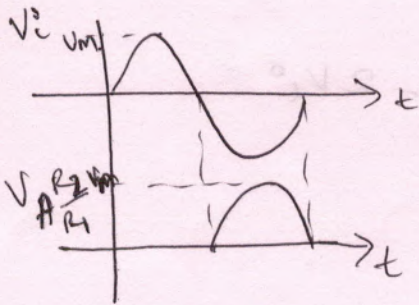D_1 is ON , D_2 is OFF

$\therefore V_A = 0$

$V_B = -R_f V_i^o$

Case (ii)   During negative half-cycle

D_1 is OFF , D_2 is ON

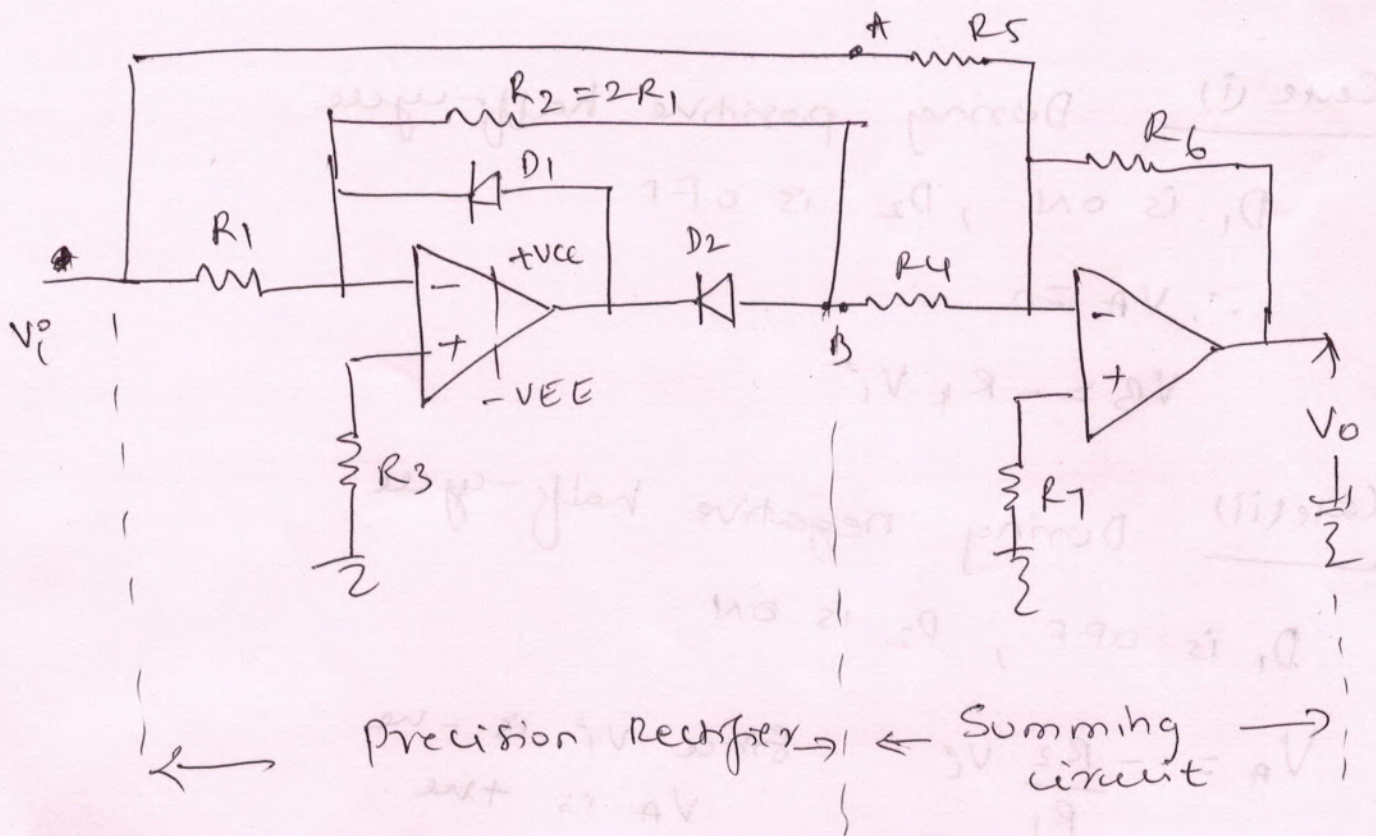$V_A = -\dfrac{R_2}{R_1} V_i$ Since V_i is -ve
                              V_A is +ve.
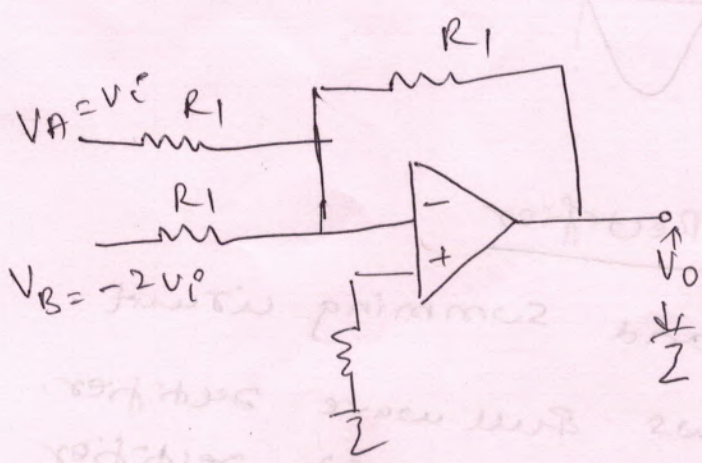
$V_B = 0$

Precision Full-wave Rectifier

1) Half-wave rectifier and summing circuit.

The fig below shows full wave rectifier.
It consists of a Half-wave precision rectifier
and an adder.

Precision Rectifier $\longrightarrow$ | $\leftarrow$ Summing circuit $\rightarrow$

Case (i) During positive half-cycle

D₁ is OFF, D₂ is ON.

$$V_B = -\frac{R_2}{R_1} V_i = -\frac{2R_1}{R_1} V_i = -2V_i$$

$V_A = V_i$

$V_B = -2V_i$

$$V_0 = -\left[\frac{R_1}{R_1} V_i + \frac{R_1}{R_1}[-2V_i]\right]$$

$$\underline{\underline{V_0 = V_i}}$$

Case (ii) During negative half-cycle

D₁ is ON, D₂ is OFF

$V_B = 0$, $V_A = V_i$

$$V_0 = \frac{-R_1}{R_1}\left[V_\rho\right] = -V_i$$

Since V_ρ is negative, V_0 is +ve.

← Slope = 1

slope = 1

Note

When R_6 is greater than R_4 and R_5 not only rectification but amplification is possible. A precision full wave rectifier is also called as an absolute value circuit.

Ex:- Design a precision Full wave rectifier circuit to produce a 2V peak output from a Sine wave input. with a peak value of 0.5V and a frequency of 1MHz. use a bipolar opamps with a supply of ±15V.

$$I_1 >> I_B(term)$$

let $I_1 = 500\mu A$ (for adequate diode current)

$$R_1 = \frac{V_1}{I_1} = \frac{0.5}{500 \times 10^{-6}} = 1k\Omega$$

$$R_2 = 2R_1 = 2k\Omega \quad [\text{use two } 1k\Omega]$$

Choose $R_4 = R_5 = R_1 = 1k\Omega$

$$R_3 = R_1 \| R_2 = 1k\Omega \| 2k\Omega = 667\Omega$$

use $R_3 = 680\Omega$

$$V_0 = \frac{R_6}{2R_1} V_i \qquad \frac{V_0}{V_i} = \frac{R_6}{R_1} = \frac{2}{0.5} = 4$$

$$R_6 = 4R_1 = 4k\Omega$$

use $R_6 = 3.9k\Omega$

$$R_7 = R_4 \| R_5 \| R_6$$
$$= 1k\Omega \| 1k\Omega \| 3.9k\Omega$$
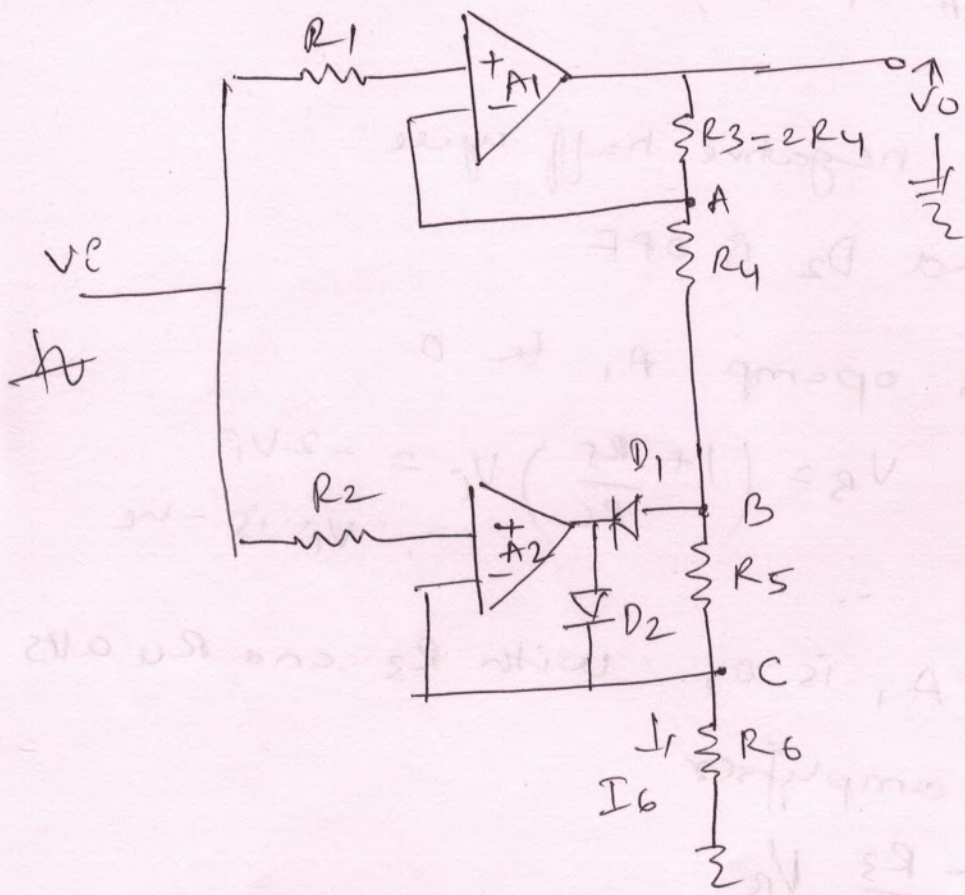$$= 443\Omega$$

use $R_7 = 430\Omega$

For diode, D_1 and D_2 the reverse breakdown voltage > 30V

$$\therefore t_{rr} < T, \quad t_{rr} = \frac{T}{10} = \frac{10^{-6}}{10} = 10^{-5} sec$$
$$= 0.1\mu s$$

High input impedance full wave precision Rectifier

A precision rectifier which uses a non-inverting configuration to present a high input impedance to the signal is shown below.

Op-amp A_1 with R_3 and R_4 and op-amp A_2 with R_5 and R_6 constitute two non-inverting amplifiers. However diodes D_1 and D_2 affect the operation of the circuit.

Case(i) During positive half-cycle D_2 is ON and D_1 is OFF.

opamp A_2 acts as Voltage follower

i. $V_O = V_i$

$V_A = V_i$

Since there is no potential difference between A and C, no current flows through R_3.

∴ drop across R_3 is 0.

∴ $V_O = V_A = V_i$

Case(ii) During negative half cycle

D_1 is ON and D_2 is OFF

let input to opamp A_1 be 0

If $R_5 = R_6$, $V_B = \left(1 + \dfrac{R_5}{R_6}\right) V_i = -2V_i$

∴ V_i is −ve

when i/p to A_1 is 0, with R_3 and R_4 acts as inverting amplifier

∴ $V_O = -\dfrac{R_3}{R_4} V_B$

If $R_3 = 2R_4$, $V_O = -2 V_B$

$V_O = -2(-2V_i) = 4 V_i$

let i/p to opamp A_2 be 0

$V_B = 0$

A_1 with R_3 and R_4 acts as non-inverting amplifier.

∴ $V_O = \left(1 + \dfrac{R_3}{R_4}\right) V_i = -3V_i$

∴ V_i is −ve

By superposition theorm

$$V_0 = +4V_i - 3V_i = V_i$$

$$\therefore V_0 = V_i$$

Hence the above circuit works as full wave rectifier with high i/p impedance.

Design v) R_6 is calculated first,

Then $R_4 = R_5 = R_6$, $R_3 = 2R_4$

Enir using Bipolar opamp with $V_{cc} = \pm 15V$, design the high input impedance precision full-wave rectifier circuit. The input peak voltage is to be 1V and no amplication to occur.

Let $I_6 = 500 \mu A$

$$R_6 = \frac{V_1}{I_6} = 2 k\Omega$$

use $R_6 = 1.8 k\Omega$

$R_4 = R_5 = R_6 = 1.8 k\Omega$,

$R_3 = 2R_4 = 3.6 k\Omega$
use two 1.8 $k\Omega$ in series

$$R_1 = R_3 \| R_4 = 3.6 k \| 1.8 k$$
$$= 1.2 k\Omega \text{ (Std value)}$$
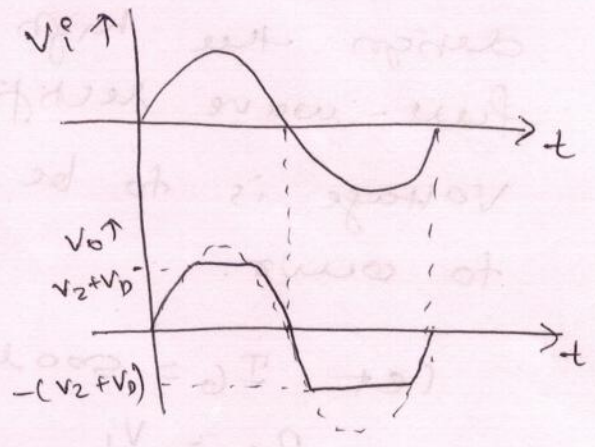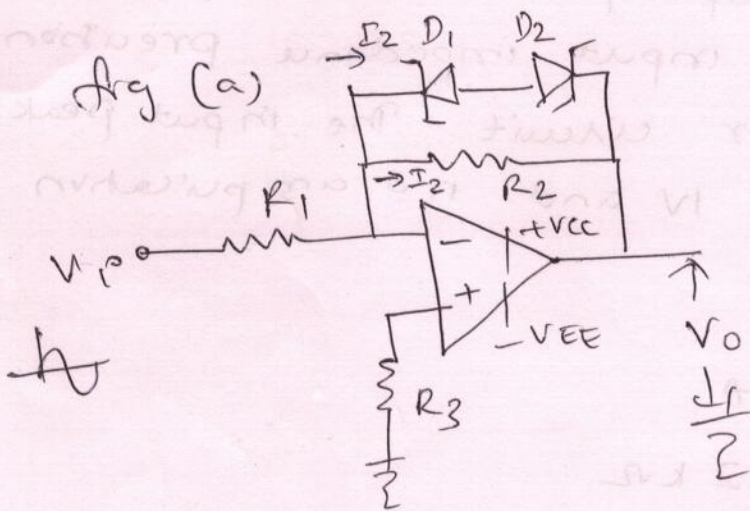
$$R_2 = R_5 \| R_6 = 1.8 k \| 1.8 k = 900\Omega$$
use $R_2 = \dfrac{1 k\Omega}{2}$ std value.

Limiting circuits

Peak clipper

The fig below shows the circuit of a peak clipper where back to back zener diodes are used to clip the peaks of the input at the output. One diode is forward biased (V_d), and the other is driven into breakdown (V_z), when the o/p voltage is greater than $(V_D + V_z)$.

The o/p cannot exceed $\pm (V_D + V_z)$.

fig (a)

As long as $|V_0| < |V_z + V_D|$, the circuit behaves as a inverting amplifier. This type of circuit is used to protect a device that might be damaged by excessive input voltage.

The fig (b) shows a resistor R_4 connected in series with R_1, so that output limiting voltage can be adjusted.

Zener diodes are connected to the moving contact of R_4.

let $\quad V_2 + V_D = V_0 \text{ Max} = \pm 14V$

$$R_1 = R_2 = R_4$$

with a moving contact at right side of R_4

$$V_0 (\text{Max}) = V_2 + V_D = \pm 14V$$

At left side of R_4, $\quad V_0 = V_{R_2} + V_{R_4} = V_2 + V_D = \pm 14V$.

with $R_2 = R_4$, $\quad V_{R_2} = V_{R_4} = \pm 2V$

By means of moving contact, the maximum output voltage can be adjusted between $\pm 2V$ to $\pm 4V$.

In general if $R_2 = R_4$, output clipping voltage can be adjusted between $\pm (V_D + V_2)$ and $\pm \left(\dfrac{V_D + V_2}{2} \right)$

The circuit voltage gain remains $-\dfrac{R_2}{R_1 + R_4}$
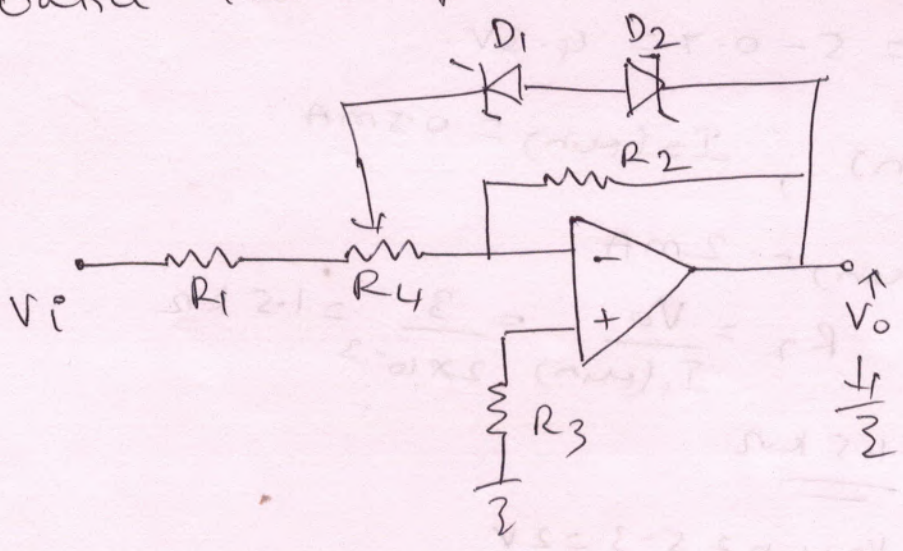
until the o/p limit is used.

fig (b)

Design :- Zener diodes are selected to limit the output voltage at the desired level with $V_D = 0.7V$.

The Inverting amplifier is designed to produce the desired voltage gain.

when the o/p reaches the limiting level current flowing through R_1, part of it flows through R_2 and part through Zener diodes,

$$I_{R_1} > 0.5mA .$$

prob Design an adjustable clipping circuit as in fig (6) to clip at approximately $\pm(3V \text{ to } 5V)$. The circuit is to have unity voltage gain before clipping.

$$V_{O(Max)} = V_Z + V_D = 5V$$

$$V_Z = 5 - 0.7 = 4.3V.$$

$$I_1 > I_Z(Min) , \qquad I_Z(Min) = 0.5mA .$$

let $I_1(Min) = 2mA.$

for $V_O = 3V, \qquad R_2 = \dfrac{V_O}{I_1(Min)} = \dfrac{3}{2 \times 10^{-3}} = 1.5 k\Omega$

$$R_2 = 1.5 k\Omega$$

$$V_{R_4} = V_{O \, Max} - V_{O \, Min} = 5 - 3 = 2V$$

$$R_4 = \dfrac{2}{2 \times 10^{-3}} = \dfrac{1 k\Omega}{2} = 1 k\Omega \text{ variable pot.}$$

for $A_V = 1$, $R_1 + R_4 = R_2$, $R_1 = R_2 - R_4 = 0.5K.$

we $R_1 = 470\Omega$, $\qquad R_3 = (R_1 + R_4) \| R_2$

$$R_3 = 1.47 K \| 1.5 k = 742 \Omega$$

we $R_3 = 680 \Omega$

Dead Zone circuit

A dead zone circuit can be obtained by adding a resistor R_1 and a dc reference voltage V_{ref} to half-wave precision rectifier. This is shown in fig below.

If R_1 and V_{ref} were absent, the circuit behaves as an inverted half-wave precision rectifier.

If diodes were absent (D_1 OFF, D_2 ON) the circuit behaves as an inverting summing circuit output of $V_0 = -(V_{ref} + V_i)$

(i) Let V_{ref} be positive

when $V_i = 0$, V_0^1 is -ve $\therefore D_1$ is ON D_2 is OFF.

and $V_0 = 0$

when V_i goes -ve and goes just below $-V_{ref}$ V_0^1 becomes +ve, so that D_1 is OFF D_2 is ON.

ie $\ell V_i) = |+V_{ref}|$, $V_0 = 0$ and o/p, $V_0 = -(V_{ref} + V_i)$

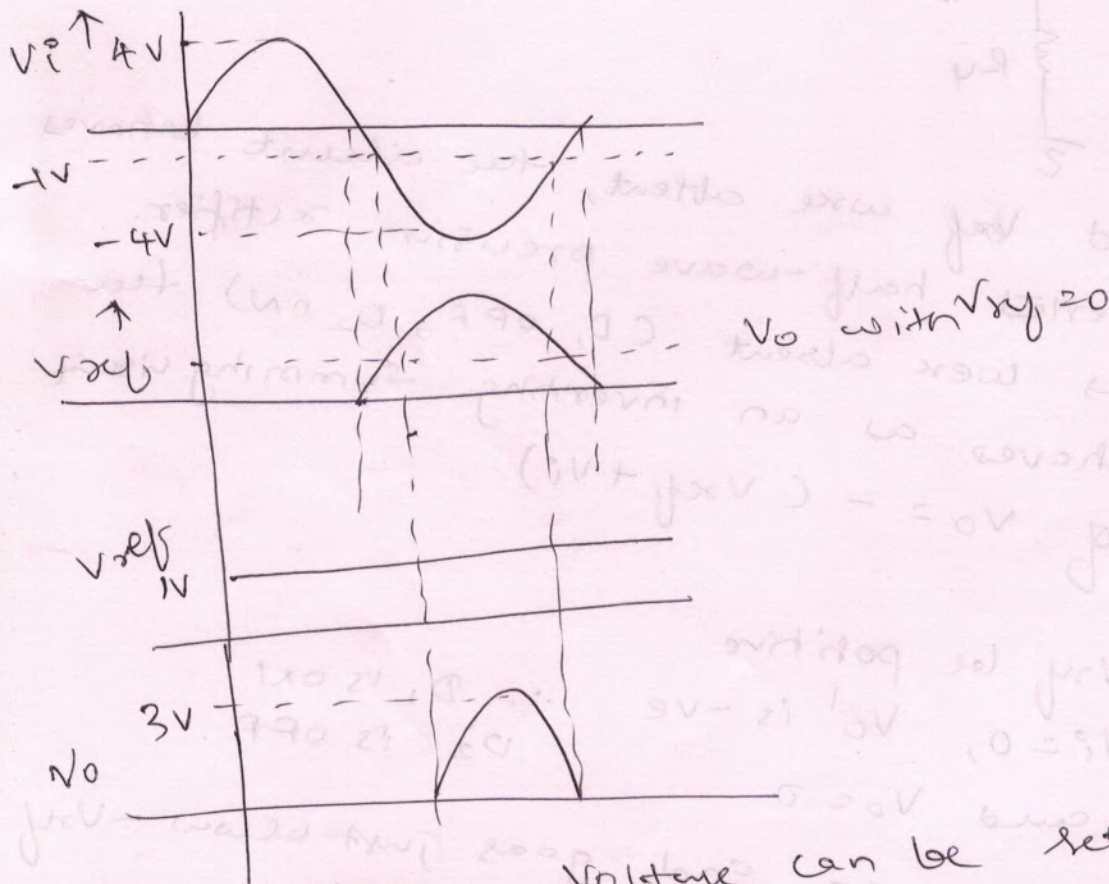since V_i is -ve, $V_0 = -V_{ref} + V_i$

Ex:- let $V_{ref} = +1V$

when $V_i > -1V$, D_1 is ON, D_2 is OFF & $V_0 = 0$

when $V_i < -1V$, Say $V_i = -4V$

$$V_0 = -1 + 4 = 3V$$

The circuit o/p remains 0 until $(-V_i) > (+V_{ref})$

when $(-V_i) > (+V_{ref})$, o/p follows the input. The ineffective portion of the input are said to occupy a dead zone.

V_0 with $V_{ref} = 0$

The reference voltage can be set to any convenient level, positive or negative and can be made adjustable. If the polarity of diodes and V_{ref} are reversed, the circuit produces an inverted version of the positive o/p peak. Instead of V_{ref} is adjustable R_1 can be made adjustable.

Ex:- Using a BIFET opamp design a dead zone circuit to pass only the upper 1V portion of the positive half-cycle of the sine wave i/p with a peak value of 3V.

$$V_{ref} = V_0 - 1 = 3 - 1 = 2V.$$

$$I_{R_1}(min) = I_0(min) = 500 \mu A$$

$$I_{R_1} R_1 = 2$$

$$R_1 = \frac{2}{500 \times 10^{-6}} = 4K, \quad \text{use } R_1 = 3.9 k\Omega.$$

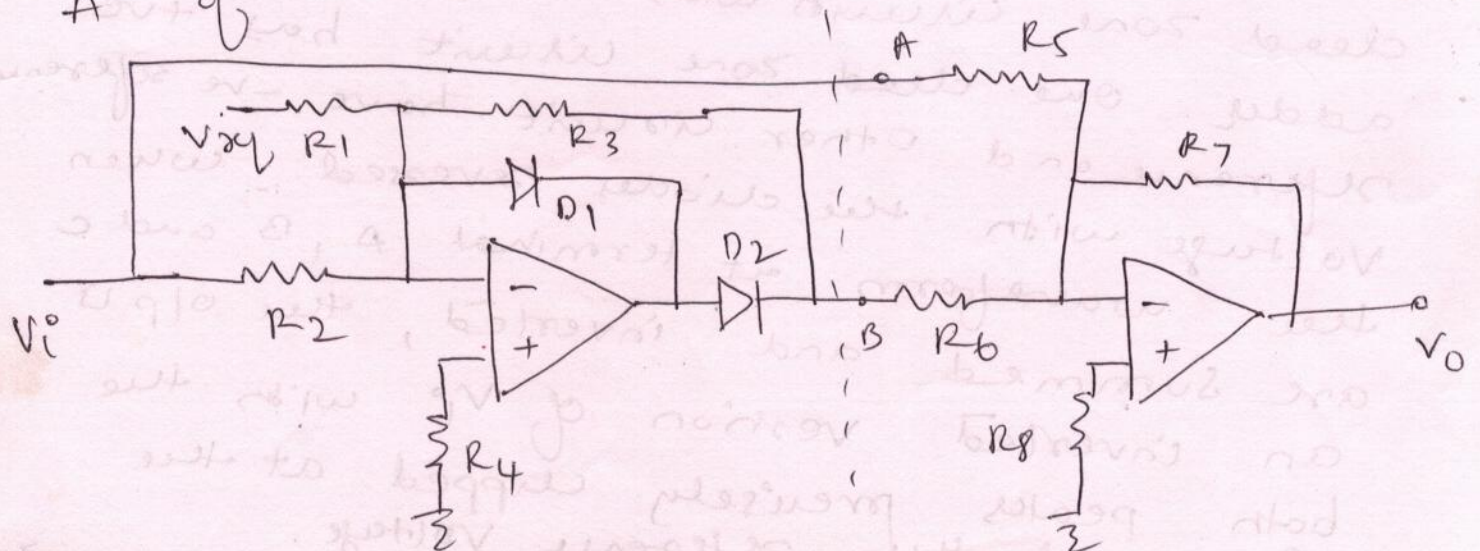$$R_1 = R_2 = R_3 = 3.9 k\Omega$$

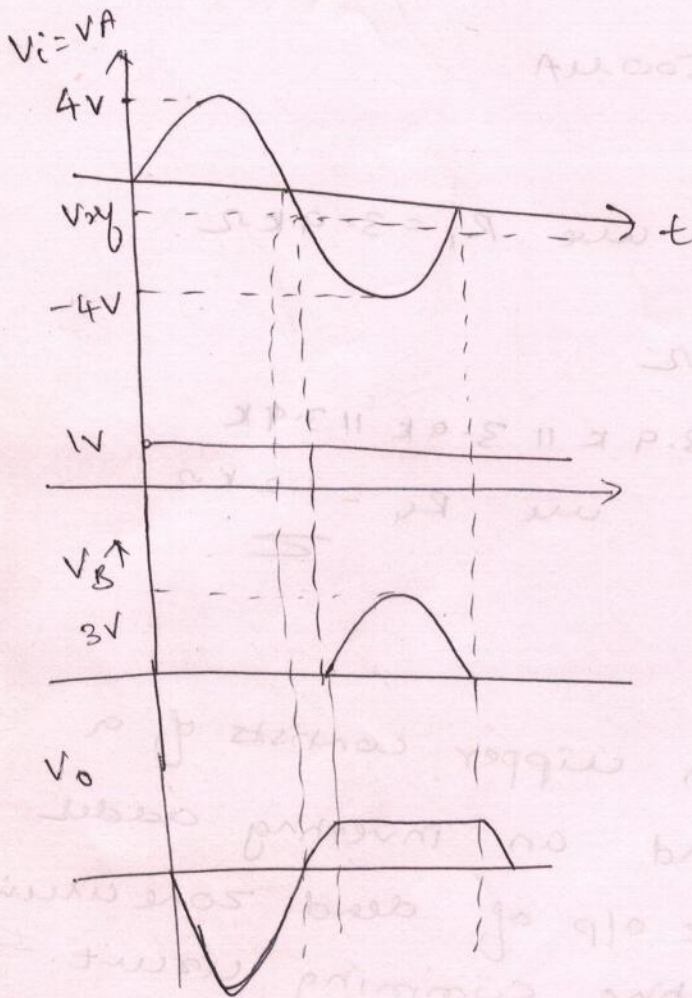$$R_4 = R_1 \| R_2 \| R_3 = 3.9 K \| 3.9 K \| 3.9 K$$

$$R_4 = 1.3 k\Omega \quad \text{use } R_4 = 1.2 k\Omega$$

Precision clipper

A precision clipper consists of a dead zone circuit and an inverting adder as shown in fig. The o/p of dead zone circuit is applied to an inverting summing circuit. The i/p v_i is applied at terminal (terminal B). The i/p v_i is applied at terminal A of the summing circuit.

The waveforms at terminals A and B resultant o/p V_0 is shown. The o/p is inverted i/p w/f with the positive peak precisely clipped off above the level of V_{ref}.

The waveforms at terminal A and B.

The fig below shows the symmetrical precision clipping circuit. It consists of two dead zone circuits with a 3 i/p inverting adder. One dead zone circuit has +ve reference and other circuit have -ve reference voltage with the diodes reversed. when the waveform at terminal A, B and c are summed and inverted, the o/p is an inverted version of V_i with the both peaks precisely clipped at the reference voltage.
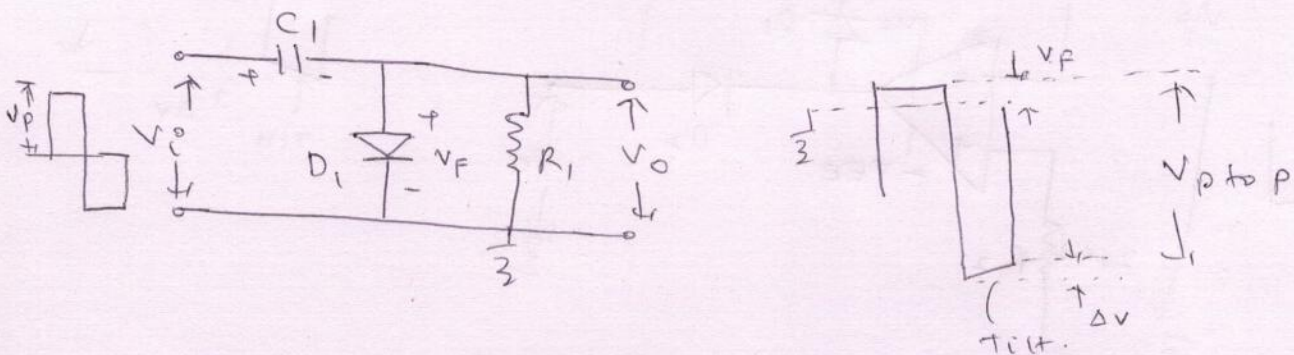
* clamping circuits

Diode clamping circuit

A clamping circuit reproduces an input waveform without any clipping or distortion, but limits the upper or lower peak of the waveform to a predetermined level.

Consider the diode clamping circuit shown in fig,

Tilt.

when the input voltage is positive, diode D_1 is forward-biased and capacitor C_1 changes with the polarity shown.

The peak input voltage (V_p) appears across C_1 and D_1 so the capacitor charges to

$$V_{C_1} = V_p - V_F$$

At this time, the output voltage cannot exceed the voltage drop across the forward biased diode.

$$\therefore V_0 = V_F.$$

when the input goes to its negative peak, D_1 is reverse biased and input and capacitor voltages combine to produce an output of
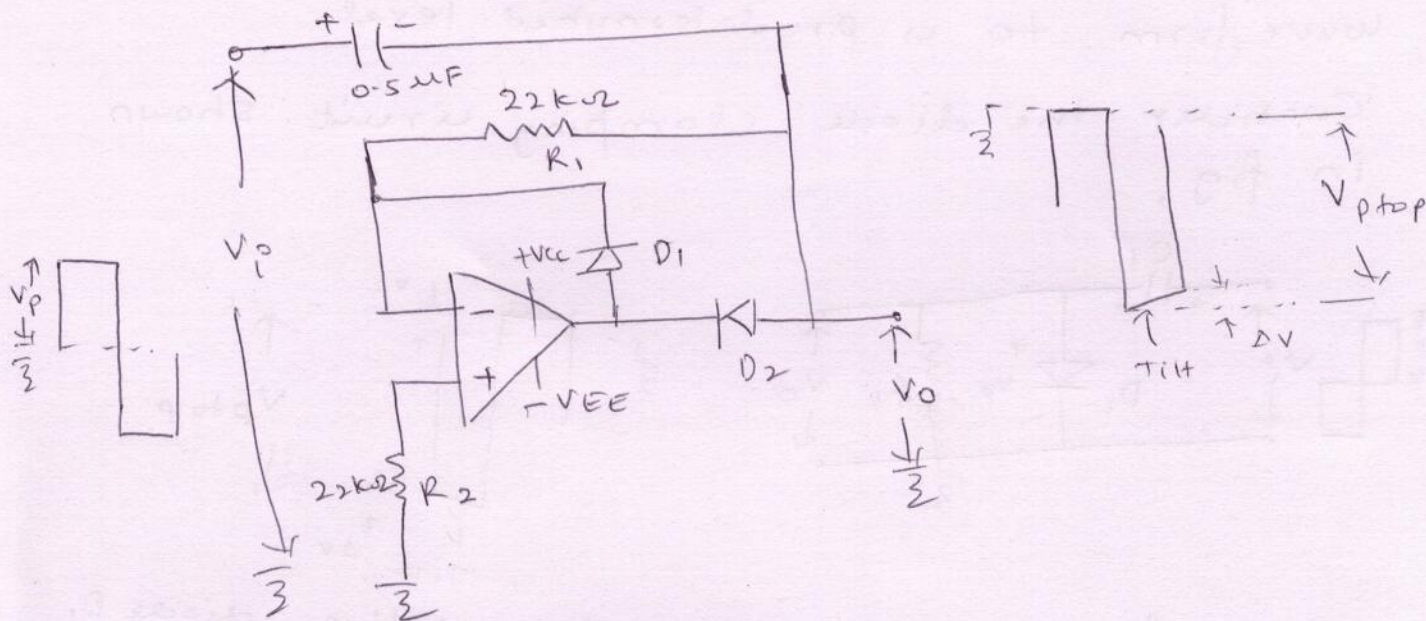
$$V_0 = -V_p - V_{C_1}$$
$$V_0 = -V_p - (V_p - V_F)$$
$$V_0 = -2V_p + V_F$$

The Resistor R_1 is used to ensure the capacitor discharges when the peak input voltage drops to a lower level. R_1 produces tilt (or slope) on the unclamped peak of the output.

precision clamping circuit.

The precision clamping circuit is shown above.

When the input voltage is at $+V_p$, the circuit output tends to move in positive direction. Thus, because the op-amp inverting input is connected to the output by resistor R_1, the inverting input terminal tends to be positive with respect to the grounded non-inverting input terminal. This causes the op-amp output to go negative, resulting in diode D_2 being forward biased and diode D_1 being reverse biased. Negative feedback via R_1 keeps the inverting input terminal and the anode of D_2 within μV of ground level.

The output voltage at this time is
$$V_0 = 0.$$

when the input goes to its negative peak, the circuit output and the op-amp inverting input terminal tend to go negative. The Negative voltage at the inverting input causes the op-amp output terminal to move in positive direction, reversing D_2 & forward biasing D_1. Now, negative feedback via D_1, keeps the op-amp inverting input terminal close to the level & the grounded non-inverting input terminal. With D_2 reverse biased, the circuit output is completely free to move in a negative direction, giving the output &,

$$V_0 = V_i + V_{c_1}$$

$$V_0 = -V_p + (-V_p)$$

$$V_0 = -2V_p.$$

Reversing the polarity & D_1 and D_2 produces Clamping & the lower level & the output waveform.

In any clamping circuit, the signal source resistance R_s is in series with the capacitor when it's charging. Allowing that the capacitor should be completely charged from zero to V_p in five cycles & i/p waveform,

$$5 C_1 R_s = 5 \times \frac{T}{2}, \quad \text{where } T = \text{time period & waveform.}$$

$$\therefore \quad C_1 = \frac{T}{2R_s} = \frac{1}{2R_s f}.$$

when C_1 is discharging via R_1, the voltage across R_1 is

$$V_0 = 2 V_P$$

giving a discharge current of

$$I = \frac{2 V_P}{R_1}$$

and

$$C_1 = \frac{Q}{\Delta V} = \frac{I t}{\Delta V}$$

where ΔV is the discharge voltage, or tilt, on the unclamped peak and t is the discharge time $T/2$.

$$\therefore \quad C_1 = \frac{2 V_P}{R_1} \times \frac{T}{2} \times \frac{1}{\Delta V}$$

$$\therefore \quad R_1 = \frac{V_P}{C_1 \Delta V f}$$

prob A $\pm 5v$, 10 KHz Square wave from a signal source, with a resistance of 100Ω is to have its positive peak clamped precisely at ground level. Tilt on the output is not to exceed 1% of peak amplitude of wave. Design a suitable op-amp precision clamping circuit with supply of $\pm 12V$.

$$C_1 = \frac{1}{2 R_s f} = \frac{1}{2 \times 100 \times 10 \times 10^3} = 0.5 \mu F \ (std).$$

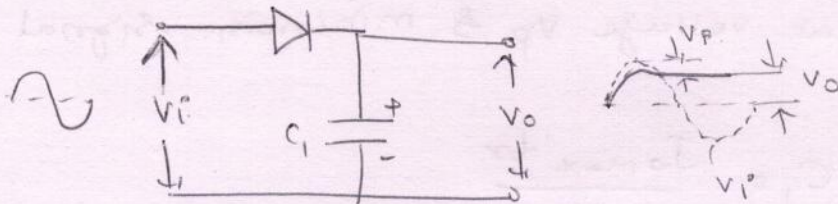$$\Delta V = 1\% \ \text{of} \ 5v = 0.05 v$$

$$R_1 = \frac{V_P}{C_1 \Delta V f} = 20 k\Omega = 22 k\Omega.$$

$$R_1 = R_2 = 22 k\Omega$$

Peak Detectors :

A peak detector monitors an input signal and holds its output voltage at the peak level of the input.
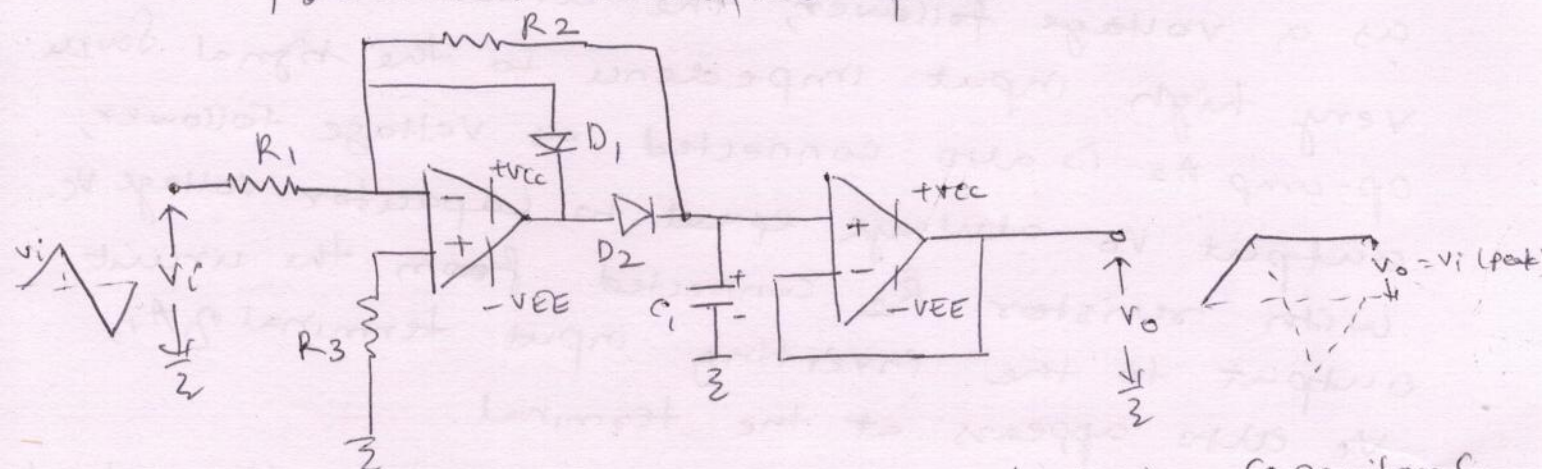
a) Simple diode capacitor peak detector.

when the input voltage increases to V_P, the Capacitor is charged to $(V_P - V_F)$. when V_i falls below V_P, D_1 is reverse biased and C_1 retains its charge.

The drawback of the above circuit is that the diode voltage drop introduces considerable error.

b) Precision rectifier peak detector.

In the above circuit, holding Capacitor C_1 is charged via low-output resistance of op-amp A_1. By making resistor R_2 greater than R_1, the signal may be amplified as well as peak detected. op-amp A_2 connected as voltage-follower

isolates the capacitor from the discharging effect of any load resistance.

WKT
$$C = \frac{Q}{V} = \frac{I \cdot t}{V} = \frac{I_d \, t_h}{\Delta V}$$

$$C_1 = \frac{I_d \, t_h}{\Delta V}$$

I_d = discharge current

t_h = holding time

ΔV = capacitor discharge voltage

For a peak voltage V_p & minimum signal rise time t_r,

$$C_1 = \frac{I_{o max} \, t_r}{V_p}$$

$$I_{o max} = \frac{C_1 \, V_p}{t_r} \quad , \quad \text{Min. slew rate} = 3 \frac{V_p}{t_r}$$
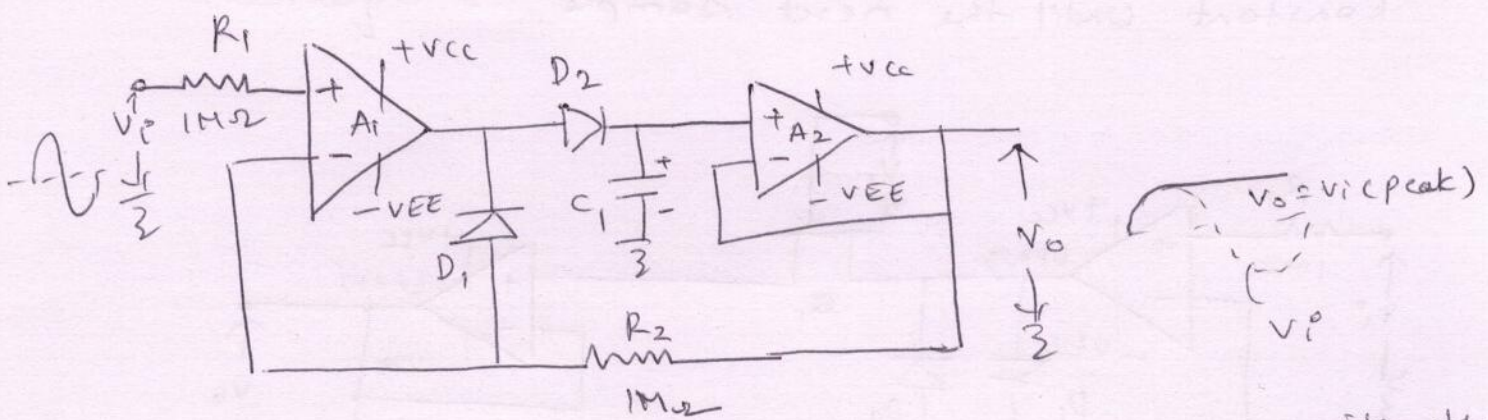
Voltage Follower peak detector

In the ~~previous~~ circuit, the only Capacitor discharge currents are the input bias current to op-amp A_2 and reverse leakage current of diode D_2. As op-amp A_1 is connected as a voltage follower, the circuit presents a very high input impedence to the signal source. op-amp A_2 is also connected as voltage follower, output v_o always equal to capacitor voltage V_c. with resistor R_2 connected from the circuit output to the inverting input terminal of A_1, V_c also appears at the terminal.

When v_i is greater than V_c, the output & A_1 is positive, D_2 is forward biased and A_1 behaves as a voltage follower, charging C_1 to V_p. when v_i falls below V_p, V_c remains at V_p, & consequently, the inverting input terminal of A_1 also remains at V_p. ∴ the output &

op-amp A_1 goes negative, reversing D_2 and forward biasing D_1. Negative feedback via D_1 keeps A_1 from going into saturation.

prob : Design voltage follower peak detector with the pulse-type signal voltage has a peak value approximately 2.5V with a rise time of 5us, and o/p voltage is to be held at 2.5V for a time of 100us. The maximum output error is to be approximately 1%. Calculate the required component values and specify the o/p current and Slew rate of op-amp.

$\rightarrow$ use BIFET op-amps for mini capacitor leakage current.

let $R_1 = R_2 = 1M\Omega$

C_1 discharge current, $I_d \approx I_r(D_2) = 1\mu A$

$\Delta v = 1\% \text{ of } V_P = 1\% \text{ of } 2.5 = 25mv$
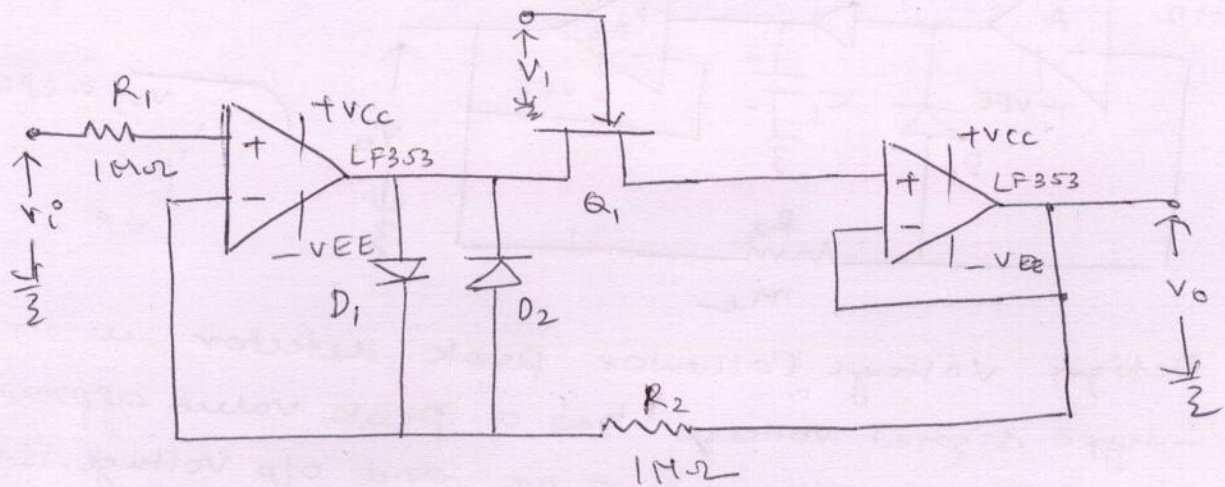
$C_1 = \dfrac{I_d \, t_h}{\Delta v} = 4000 \, pf \text{ (std)}$

For Opamp A1, $I_o(max) = \dfrac{C_1 V_P}{t_r} = \dfrac{4000PF \times 2.5v}{5us}$

$= 2 mA$.
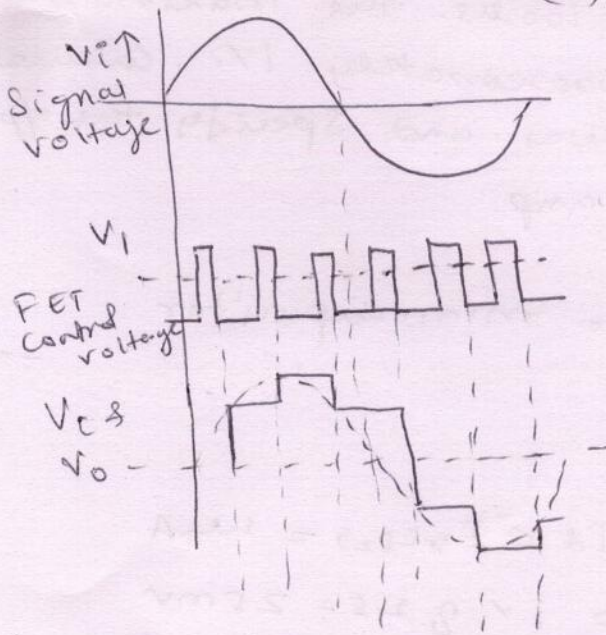
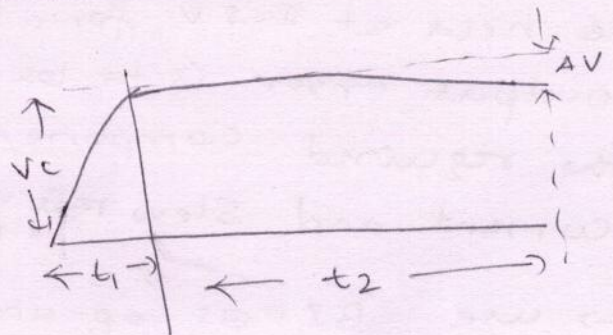min. slew rate $= 3\dfrac{V_P}{t_r} = 1.5 \, V/us$

* Sample and Hold circuits.

A Sample and Hold ciruit Samples amplitudes of a signal voltage at any point in its waveform and holds the voltage level Constant until the next sample is aquired.

(a) Sample and Hold ciruit.

(b) w/f

(c) Capacitor voltage.

Q_1 is repeatedly switched ON and OFF by the pulse waveform (control voltage V_1) applied to its gate terminal. If input v_i becomes larger than Capacitor voltage V_c while Q_1 is OFF, C_1 rapidly charges to the level $f v_i$ when Q_1 switches ON. If V_c is initially greater than v_i, C_1 is

c_1 is discharged to the level of v_i when Q_1 is ON. When Q_1 is OFF, only the input bias current to A_2 and the FET gate-source reverse leakage current are effective in discharging the capacitor. So, C_1 holds the sampled voltage constant until the next sampling instant.

During the sampling time or acquisition time, C_1 is charged via the FET channel resistance $R_{D(ON)}$. If the sampling time is

$$t_1 = 5 C R_{D(ON)}$$

the capacitor is charged to 0.993 of the input voltage, resulting in a 0.7% error in the sample amplitude.

If $t_1 = 7 C R_{D(ON)}$ is used error is 0.1%.

During the holding time t_2, the capacitor is partially discharged.